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DesignCon 2003
**High-Performance System Design**

# IC Package Design's Effects on Signal Integrity

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# Abstract
# IC Package Design's Effects on Signal Integrity


Integrated Circuit packages have several functions. They protect the IC, allow interconnection between the IC and the board, and provide a path for thermal conduction away from the IC. IC device end users also often consider other package aspects. From a manufacturing perspective, how the package affects the ease of board assembly is important. For system layout and design, the package size is often a concern.

As system signal speeds progressively increase, an additional package consideration is moving to the forefront, the effects of the package on signal integrity and performance.
Will the same IC design in a different package have different signal behavior? If signal behavior is different between package types, how will it affect system performance? At what frequencies do these effects become a concern? How should system designers take package differences into account?

This paper will cover the effects of package design on signal performance. Reviewing package structures and how package design effects IC signals.

This paper will examine the performance differences between the same IC type in different packages. A laboratory comparison of a device type packaged in Thin Shrink Small Outline Package (TSSOP) and Ball Grid Array package (BGA) will be used to illustrate signal performance differences.

The paper will also outline modeling methods for understand packaging effects on IC signal performance.


## Author Biography


Sean Clark is a Senior Applications Engineer at Fairchild Semiconductor with over 18 years experience in the semiconductor industry. His recent publications include articles and papers on BGA packages, and High Speed Signal Integrity.

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# IC Package Designs and IC Signal Performance

IC packages have a significant effect on the performance of the device. As system frequency and edge rate speeds increase, package effects become more significant. Furthermore, package design and construction vary significantly. The same IC device in two different packages can have two very different performance characteristics.

By understanding package structure and how a package affects device performance, engineers are better equipped to anticipate and prevent potential system problems. Understanding packaging effects is particularly important when migrating from one package to another.

## *A review of package structures*

The device package performs a complex function. A package is designed to protect the die, distribute power and signals, and also must dissipate device generated heat. Package structures vary considerably. Consequently how well a package protects a device and dissipates heat, as well as how it affects IC performance can vary significantly between package designs.

### SOIC

Small Outline IC (SOIC) and variants such as Thin Shrink Small Outline Package (TSSOP) use the same basic construction. These packages start with a lead frame, ordinarily made of tin plated copper. The die is bonded to the center paddle of the lead frame, usually with a conductive adhesive, and the die bond pads are wire bonded to the appropriate lead frame locations. The assembly is then injection molded with a special package mold compound. The completed package protects the assembly from damage, but is not hermetically sealed.

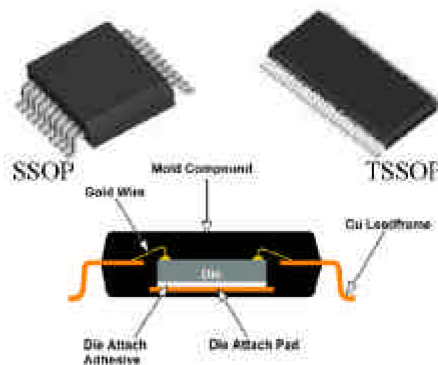


Figure 1 Illustration of SSOP and TSSOP packages and a package cross section.

### PLCC

Chip Carriers such as Plastic Leaded Chip Carrier (PLCC) and Quad Flat Pack (QFP) are quad packages that contain a die and connections on four sides. Construction is similar to SOIC packages. The interior is a lead frame and the exterior is commonly injection molded compound. Some designs use a pre-molded package, with

the top filled in after die attach. Some designs use ceramic instead of mold compound, although ceramic is primarily used for military or aerospace applications.

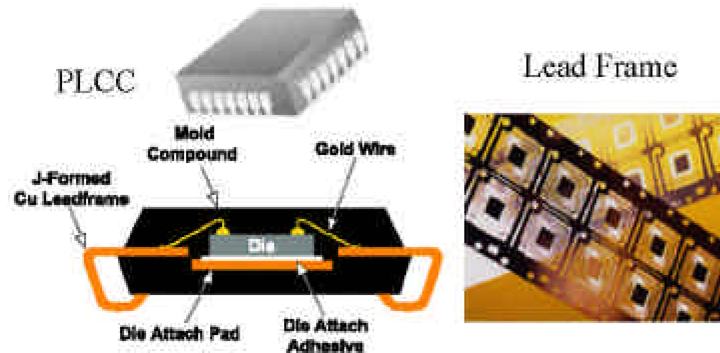


Figure 2 Illustration of a PLCC package, lead frame strip, and a package cross section.

### PGA

Pin Grid Array (PGA) packages have been used for high pin count device packages for many years. Construction is similar to that of Chip Carriers, in that the die is bonded to a lead frame. Most PGA packages are pre-molded with a package cap or encapsulant filler added after the die attach process. PGA have the advantage of socketability.

### BGA

Ball Grid Array (BGA) packages use a substrate instead of a lead frame. The substrate is not unlike a miniature P.C. board: complete with bonding contact points, traces, vias, and a non-conductive substrate material. The die is attached and bonded to the substrate. The substrate die assembly is typically covered by injection molding, similar to leaded packages. Although covering with low pressure encapsulant and ceramic packages are also sometimes used. Die can be attached to the bottom or top of the substrate material.

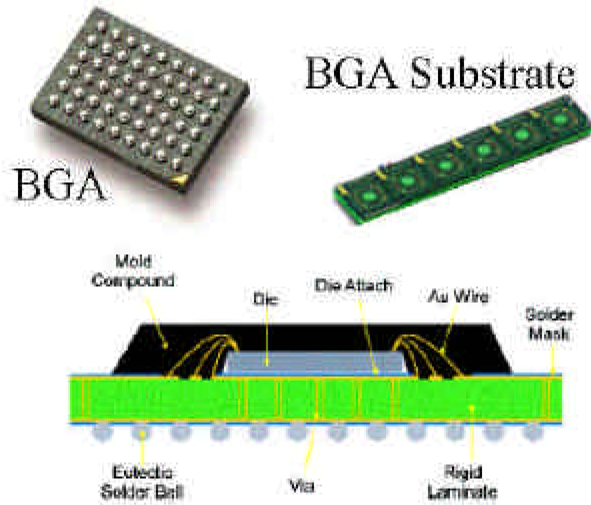


Figure 3 Illustration of a BGA device, substrate and an assembly cross section.

**Chip On Board**

Chip On Board (COB) uses the simplest construction. The die is attached directly to the circuit board with an adhesive. The die is wire bonded directly to the circuit board leads, and the assembly of wire bonds and die is covered in by a encapsulant sealant compound. The device or a subassembly of multiple COB devices may be further protected with a cover. This is one of the least expensive packaging methods. However, due to the need for low pressure encapsulant deposit, this method has a lower level of coefficient of thermal expansion (CTE) than other methods and therefore, can be less reliable than a conventionally packaged device.

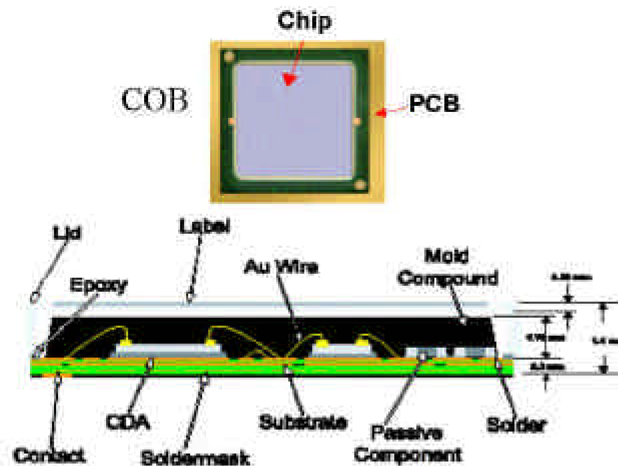


Figure 4 Illustration of a COB and an assembly cross section.

**Flip Chip**

Flip Chip devices are IC die that are 'Flipped' upside down and attached to a substrate or directly to the PC board. Many flip-chips include an intermediate package (such as BGA) to resolve issues with coefficient of

thermal expansion (CTE) and to increase the pad/ball pitch for ease of manufacture. Flip Chips use solder balls for assembly, eliminating bond wires. Flip chips also allow the direct connection of bond pads throughout the die surface to connections on the substrate or board. The use of connections throughout the die surface can significantly reduce IC die size compared to traditional 'periphery' bond pad IC connections.

The Flip Chip assembly substrates or PC board connections contain a metal bond and trace layout that is a mirror of the die bond out. Solder balls are attached to the die, and the die is 'Flipped' upside down for connection. Flip Chips may not use a package, and may not use an ecapsulant overfill, but flip chips require an 'underfill' compound to reduce CTE related stress on the solder joints. When flip chips are connected directly to the board, the finished assembly mount is only the die and hence no bigger than absolutely necessary. However, for reliable connections the die and board must have the same CTE, otherwise the solder balls will crack.

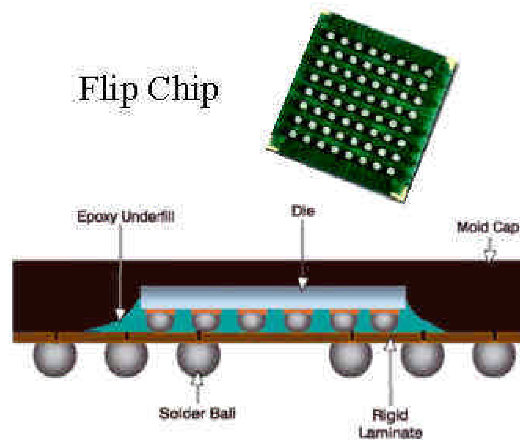


Figure 5 Illustration of a Flip Chip device and an assembly cross section.

**MLP**

Micro Lead frame Package (MLP) also known as Quad Flat No lead (QFN) are very small or near chip scale plastic packages. The design is similar to conventional SOIC in that the package consists of a lead frame with a die paddle, the die is attached to the paddle and is wire bonded to the package lead frame. However, MLP lead frames have some important differences from more conventional packages. The MLP lead frame consists of only a pad that connects the bond wire to the package exterior. In addition, when the assembly is injection molded, the package paddle is left exposed in most MLP package designs.

The very short package leads reduce the overall package footprint required. These very short leads can also enhance signal integrity in comparison to a conventional package lead finger by the minimization pin to pin capactive coupling, and the reduction of lead inductance and resistance. The exposed die paddle improves thermal conductivity. Depending upon the die function and package, package bonds are on two or four sides. Some designs use a 'flip chip' type assembly between die and package frame to achieve CSP dimensions.

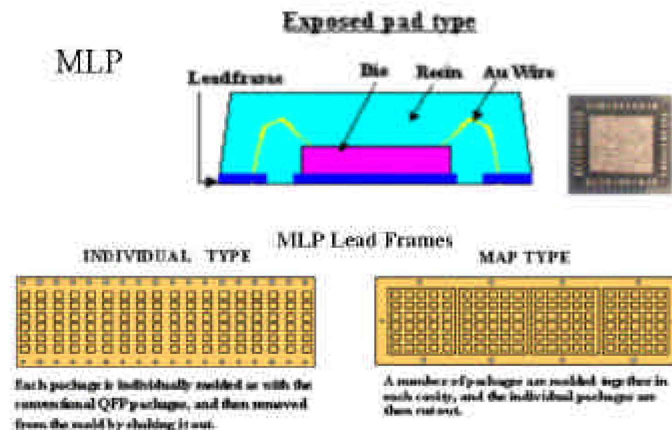


Figure 6 Illustration of a MLP device, lead frames, and an assembly cross section.

### Chip Scale Packaging

Chip Scale Packaging (CSP) is more a definition than a specific technology. The accepted definition of CSP is a package that is no greater than 20% larger than the die size. Any package and die combination that meets this definition is a CSP.

## *How package design affects I.C. signals*

A device package unfortunately is not a transparent connection between the IC die and the outside world. All packages have electrical properties that effect the performance of the IC. These properties are in the form of parasitic elements. Package parasitic elements include capacitive coupling between connections or leads, and inductive and resistive value of the connections or leads. The values of these elements have an observable and significant effect on the overall IC performance. The package layout and structure define the values of the parasitic elements.

The impact of a package on IC performance increases as edge rate speeds increase [$V = L(di/dt)$].
Package parasitic induced effects on the signal can include wave shape and device performance effects such as ground bounce and noise, propagation delay, edge rate, frequency response, and output pin skew.

### Ground Bounce

Ground bounce of a digital electronic device is the dynamic voltage level shift of the IC device ground and $V_{CC}$ during dynamic switching conditions. Ground bounce is the most visible and direct effect of the package upon device performance and output waveform. Ground bounce causes shifts in the device internal threshold and generates noise on the output signal. Ground bounce magnitude effects system noise margin and maximum reliable operation frequency of an application.

IC Package design, IC device design and system circuit design and layout all are factors in the amount of ground bounce generated in a system. In most cases, the IC package design is the largest contributor to device ground bounce. This is especially true with conventional lead frame design packages, the IC package leads behave as inductive elements during dynamic switching. These inductive elements resist the changes in current flow that are required during device switching. Figure 7 illustrates a simplified model of a CMOS device in a

package. L1 represents the inductance of the ground lead, L2 represents the $V_{CC}$ lead, and L3 the output lead. R1 represents the impedance of the output structure during a discharge of the load. CL and RL represent the output load.

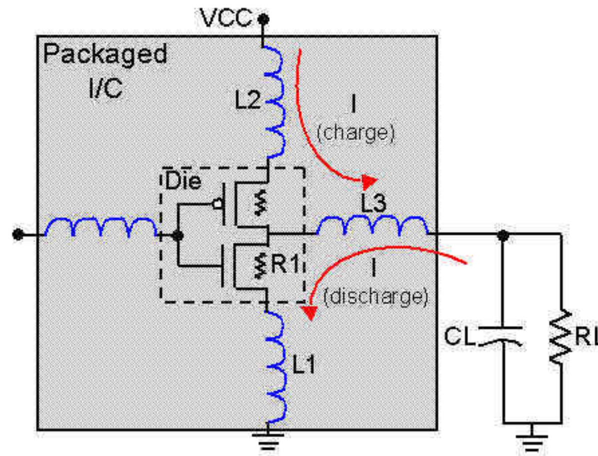


Figure 7 Simplified package and IC model illustrating inductive effects of the package leads.

To change the output load voltage level from a high to low, current flows from the output load, through the device output structure to ground. As the current changes, voltage is generated across the inductive elements of the circuit. The formula for voltage across an inductor is:

$$V = L\,(di/dt)$$

Where:

V = generated voltage
L = Inductance
di = change in current
dt = change in time

The output edge rate, and hence load discharge rate is primarily determined by a combination of package lead inductance (L1 and L3), the internal characteristics of the output transistor (R1), and the load.

The inductance (L1) between system ground and internal device ground induces a voltage as current flow changes. This induced voltage becomes the ground reference for the device. The result is a momentary voltage difference between device ground and system ground. This dynamically induced voltage creates what is known as ground bounce.

This phenomena appears as a device output signal's ground "bounce" above system ground level, followed by an overshoot swing below system ground before returning to parity with the system ground. This same phenomenon occurs on the $V_{CC}$ rail. This is the inverse of ground bounce and occurs when the device drives the load from low to high.

The effects of ground bounce are seen both as output noise and as an internal shift of the input threshold region of the device. Both the output noise and the input threshold shift of a device can greatly reduce the effective usable device noise margin.

Ground bounce magnitude is affected by several contributing factors: the number of outputs switching, output edge rate, the location of the output pin in the package and the die, the $V_{CC}$ voltage, the load type and location, and the device technology.

The number of output pins switching in the same direction coincident with one another will affect the amplitude of the ground bounce pulse. Each output discharging a load passes this load current through the same device and package ground pins. This increases the current across the package ground leads, resulting in an increase in ground bounce magnitude.

The location of the output pin in relation to the ground and $V_{CC}$ pins also affects ground bounce. As the output pin distance from ground increases, the current discharge path length to external ground increases. This increases the resistance and inductive value of the discharge path, which in turn increases ground bounce amplitude. For this reason, increasing the number and location of ground and $V_{CC}$ die and package connections lowers ground bounce magnitude by decreasing resistance and inductance. Some designs and technologies take this a step further and include Quiet Grounds, which separate the output circuits from the rest of the device circuitry on the die, further quieting the device.

The $V_{CC}$ voltage level affects the output voltage swing and the amount of current available. A higher value $V_{CC}$ increases the value of the voltage that must change across the load, this in turn increases the magnitude of the current flow. Larger amounts of current flow contribute to increases in ground bounce.

Device technology and design also play a role in ground bounce generation. In simple terms, higher output drive devices generate steeper edge rates, and steeper edge rates generate more bounce. However there are many mitigating factors.

Higher rated device output drive is derived from increased transistor size. Larger transistors have lower internal resistance, allowing a load to be charged or discharged faster, this results in faster output edge rates. These faster changes in voltage create a larger induced current across the device and package inductive components in a shorter amount of time. The result is higher bounce amplitudes as transistor size increases.

Technology plays a large role in device edge rate. Pure CMOS devices, due to their design and behavior turn on more quickly than equivalent bipolar devices. The result is more ground bounce for CMOS devices than equivalent Bipolar devices. High drive CMOS devices are usually designed with edge rate control circuits to minimize ground bounce.

Non-saturating designs such as ECL have less ground bounce than TTL or CMOS single ended devices. Non-saturating designs never completely turn off and are never on in the full device saturation region of the device. By avoiding these two regions, the sharpest edge transitions are eliminated. Non-saturation technologies have additional benefits that help minimize noise generation and improve noise tolerance. These types of technology have very small voltage swings; 800mV is typical for ECL. Also, the output signal swing is offset from ground and $V_{CC}$ increasing noise immunity.

Load type and location in relation to the driving device also has a significant effect on ground bounce. A lumped capacitive load close to the output is a worst case load for generating ground bounce The charging or discharging of a lumped load creates a much greater change in current flow over time (di/dt) than charging or discharging a distributed load. This induces a much greater voltage across the ground or $V_{CC}$ lead inductance.

In an extreme cases, ground bounce can cause unintended switching, resulting in data errors. Driving device ground bounce can cause the false triggering of a receiver device if the output noise generated by the driver crosses the receiver's input threshold point. Ground bounce can cause the driving device to switch due to its moving internal threshold. The movement of the device internal switch point due to bounce is known as the "dynamic threshold".

**Dynamic Threshold**

Dynamic threshold is the direct result of device ground bounce. Dynamic threshold problems arise when a dynamic input threshold crosses through the static input threshold level. This will cause the device to switch, generating an unwanted change of state.

**Pin-to-Pin Capacitive Coupling and Edge Rate**

Pin-to-pin capacitive coupling has a significant impact on output signal edge rate. As an output switches from high or low, it will capacitively couple energy onto adjacent pins. In effect this adds capacitance to the output signal line and the result is a slower output edge rate. In addition, the switching pin couples energy onto adjacent pins in the form of a current spike [I=C(dv/dt)]. This energy will be seen on the adjacent pins as a voltage spike or noise when the induced current flows through an inductive or resistive load. This noise can cause unwanted state changes on a quiet output. Fast edge rates, and larger voltage swings couple more energy to adjacent pins than slower edges or smaller voltage swings.

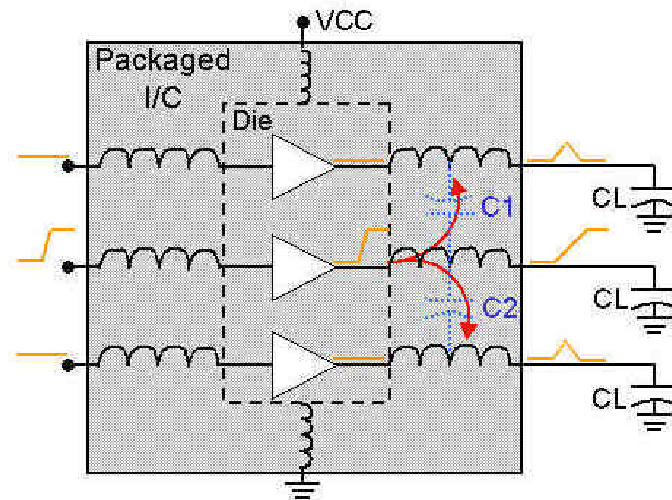


Figure 8 Simplified package and IC model illustrating pin to pin capacitive coupling.

Capacitive coupling occurs when two or more signal lines run adjacent in the package. Packages with conventional lead frames and tight lead to lead pitch are the most susceptible to pin to pin coupling.

**Frequency response**

Package frequency response is a combination of the package parasitic elements and their values, and the interaction between these elements and the IC device. As noted above, inductive elements on the $V_{CC}$ and ground leads can generate problems with bounce and output signal noise. The same inductive elements on

signal input pins will generate faster edge transitions, leading to faster switching time. Capacitive effects between I/O pins increases loading and slows edge transitions, whereas capacitance on $V_{CC}$ and ground can inhibit current starvation and bounce. All these elements have a significant effect on performance of the IC.

### Skew and Propagation Delay

Pin to pin skew and propagation delay are directly related to device design, device layout, and package construction.

The package construction can have a significant effect on skew. For example, a lead frame for a rectangular package with leads only on two sides that is combined with a square die needs very different lead frame leg lengths from the package center to the package end pins. The IC layout can overcome some of this if the die layout is rectangular instead of square, but the lead leg lengths will still not be completely uniform. Due to the potential package impact on skew, high performance devices that require very low skew such as clock drivers are often offered in four sided packages to minimize skew.

The same package design layout features and considerations affect propagation delay. To minimize skew, propagation time for some pins may be increased, while propagation time for others is decreased. Larger packages will have longer propagation time because of the increased lead lengths. In addition, signal propagation velocity is effected by the package. The amount of material in the package (its size) and the dielectric constant of the package materials affect propagation velocity. The increase in other parasitic effects is also additive. Increases in capacitive coupling will slow edge rates and increase the time to reach switching threshold.

## *New Package Design Performance Effects*

Device packaging has changed in recent years. There is a significant trend towards smaller, CSP and near CSP packages such as the MLP package. Other new package designs such as BGA are experiencing an upsurge in use. In some instances, the package is designed to improve device performance. In other cases, package design requirements may enhance device performance as an additional benefit.

New package designs reduce the parasitic effects that alter device performance and signal shape. Some of these beneficial traits are intentional, others are due to new demands on package design such as size reduction. However, it is not a given that a new package design will have reduced parasitic effects. In addition, two packages that are externally the same may not be internally the same, and can result in very different parasitic values. Hence, two externally identical packages may produce very different performance characteristics.

Features that improve package signal performance include multiple ground and power pins, short leads, and layouts that minimize capacitive coupling between pins. Multiple ground and power pins reduce inductance, reducing current starvation and ground bounce. Very short leads or solder balls reduce inductance, resistance, and line lengths, this reduces ground bounce, and at GHz speeds all of these features can help reduce the impact of line discontinuities and transmission line effects. Therefore, the shorter the leads the better, such as the package bond contacts on an MLP or the solder balls on a flip chip or BGA.

MLP packages have a very tight lead to lead pitch. However these packages also have much smaller lead frames, and utilize package solder bonds instead of external leads. The replacement of leads with solder bonds results in much shorter line lengths. The small CSP or near CSP lead frames shorten or eliminate bond wires, coupled with the absence of conventional leads, the result is a dramatic decrease in package connection line length. Line length reduction of greater than a 50% compared to a TSSOP is typical. The result of the shortened line lengths is: reduced capacitive coupling, lower lead resistance, lower inductance, and in very high speed applications this also minimizes package transmission line effects.

Most MLP packages also have an exposed die paddle for increased thermal conductivity. A lower and more even IC temperature results in a better performance as well as increased reliability.

Some Chip on Board and Flip chip layouts have the potential to improve IC signal performance because they remove the entire package and hence, the parasitic elements from the system. However, there are some potential performance issues with these technologies. In both of these designs, the substrate may not be as well connected to $V_{CC}$ or ground as it would be with a lead frame paddle or BGA flag. Potential issues include CTE problems and poor substrate connection causing IC power stability problems.

The Chip on Board still requires bond wires for attachment, bond wires contain all the parasitic elements of the lead frame, although the short length reduces inductive and resistive values in comparison to lead frames. Also, the very small bond wire cross section minimizes capacitive coupling between pins.

Flip chip layout eliminates the bond wires and the solder ball connection reduces parasitic elements to the absolute minimum. However, to increase ease of use of CSP flip chip technology, vendors sometimes use a standard die bond template or 'footprint' to increase solder ball spacing. If the actual functional die is much smaller then the footprint, a significant amount of the die metal layers are required to route signals to the bond pads. The increase in metal trace runs increases the parasitic elements associated with the metal die traces, although this is generally still low in value when compared to a lead frame.

BGA packages, which use of a substrate instead of a lead frame offer the possibility for significant improvements in performance. The substrate board can be laid out to improve package performance and in a configuration that takes advantage of device layout and performance requirements.

The substrate power and ground connections can be located close to the die which reduces inductance and resistance. Data and control connections can be laid out to minimize pin-to-pin capacitive coupling and to eliminate any line length differences, resulting in reduced skew. Careful layout achieves a package with better overall performance than packages that use lead frames. Figure 9 Illustrates a BGA substrate layout with a wide ground ring and die attach 'flag', a wide power ring, and concentric even length signal connections. Through-substrate vias for ground, power and signals, and plating tails are also visible in the layout.

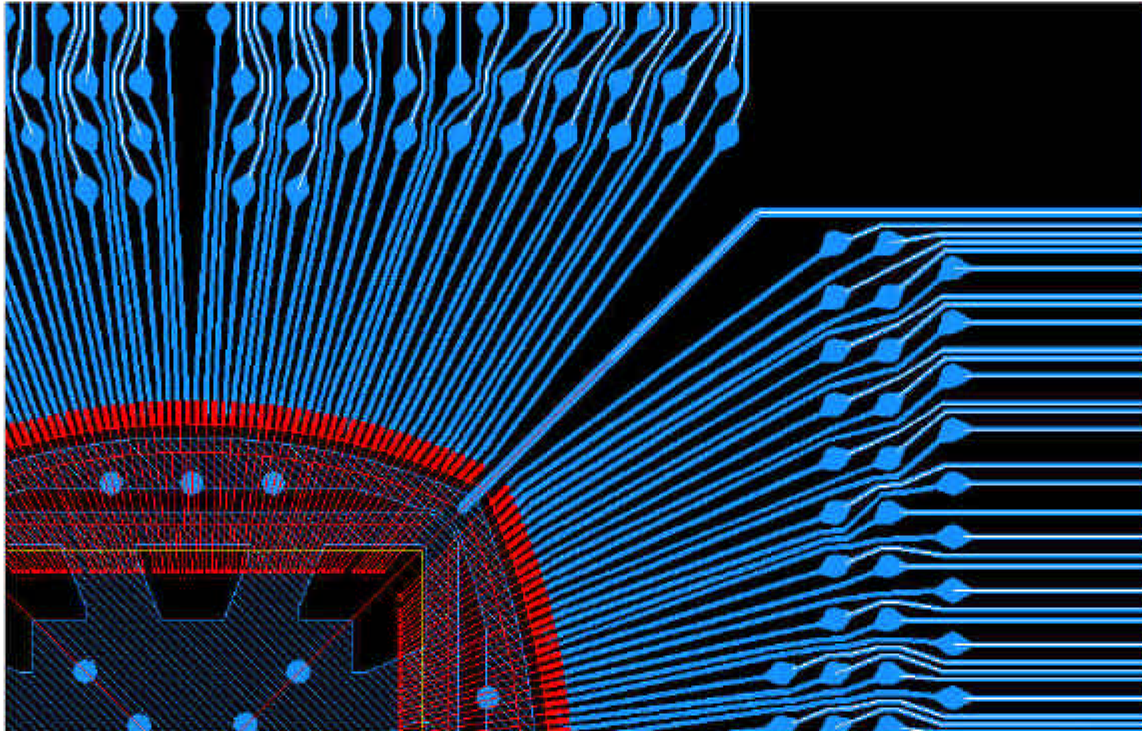

Figure 9 BGA substrate layout illustrating a layout design for maximum IC performance. (Courtesy of Synopsys Incorporated)

Not all designs take full advantage of substrate layout potential. Cost, IC complexity, and IC performance requirements factor into the decision for a custom or more generic substrate layout. However, even generic BGA packages offer some inherent advantages over lead frame packages.

BGA package designs generally have reduced parasitic pin to pin capacitance in comparison to equivalent leaded packages. Between lead capacitive coupling is usually lower than a lead frame package because the BGA substrate signal trace cross section is significantly smaller than lead frame cross section. The reduction in cross section yields a corresponding reduction in capacitive coupling. Additionally a reduction in pin to pin capacitive coupling can be achieved through careful BGA substrate layout. By reducing the distance the signal traces run parallel to each other on a BGA substrate, pin to pin capacitive coupling is further reduced.

Careful substrate layout also achieves a package with other reduced parasitic components and parasitic components that have much narrower range of distribution. Reduction of inductance and resistance on the power and ground lines reduces current fluctuations and ground bounce. Tight distributions of parasitic values for data lines reduces skew.

BGA packages may have higher capacitive coupling from output to ground plane compared to conventional leaded packages. This higher capacitance is due to the substrate manufacturing process. Plating tails are used to electroplate the substrate traces. If these tails are not removed, they act as signal stubs and increase capacitance on the traces.

| Parasitic Elements | BGA-114 | | | TSSOP-56 | | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | |
| Package Inductance | 0.73 | 2.25 | 3.96 | 1.37 | 2.42 | 4.35 | nH |
| Pin to Pin Capacitance | 0.01 | 0.06 | 0.14 | 0.11 | 0.16 | 0.32 | pF |
| Capacitance to Ground | 0.19 | 0.33 | 1.06 | 0.10 | 0.15 | 0.32 | pF |
| Package Resistance | 23 | 86 | 130 | 133 | 153 | 185 | mOhm |

| Parasitic Elements | BGA-54 | | | TSSOP-48 | | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | |
| Package Inductance | 1.92 | 2.64 | 3.47 | 1.37 | 2.14 | 3.57 | nH |
| Pin to Pin Capacitance | 0.02 | 0.06 | 0.11 | 0.11 | 0.14 | 0.27 | pF |
| Capacitance to Ground | 0.25 | 0.36 | 0.59 | 0.10 | 0.12 | 0.25 | pF |
| Package Resistance | 147 | 229 | 314 | 133 | 149 | 175 | mOhm |

Table 1 Comparison of Parasitic Elements for 2 leaded TSSOP packages and 2 BGA packages

## *Performance comparison of the same IC type in 2 packages*

To analyze and illustrate package effects on die performance and signal behavior, a laboratory evaluation was conducted on one IC design in two different package types.

The Gunning Transceiver Logic Plus (GTLP) IC device type was chosen for this test for several reasons: GTLP is a performance oriented interface technology, with typical system speeds of 33MHz to100MHz, GTLP is typically used in medium and high performance systems where signal integrity is critical to proper operation. GTLP is available in two structurally different but high use package types: the ubiquitous Thin Shrink Small Outline Package (TSSOP), and the Ball Grid Array package (BGA). Additionally, a backplane test system was available to mimic typical applications.

### Test setup

GTLP devices in 114 ball BGA and 56 pin TSSOP were evaluated side by side in a Fairchild Semiconductor lab 13 slot backplane. A photo of the backplane and test boards is shown in figure 10.

Figure 10 Photo of the evaluation backplane and test boards.

For this testing, the 13 slot backplane is configured to drive and receive GTLP signals . GTLP transceivers are designed for backplane driving, one side of the device is a CMOS TTL I/O structure. The GTLP technology side is open drain and requires a pull up resistor (RT) to a termination voltage (VT) for proper operation. GTLP signals have a typical swing of 1V peak to peak, centered around 1V. A reference voltage (VREF) is used to set the threshold switch point of the GTLP receiver, VREF is typically set to 1V.

Termination cards are connected at each end of the backplane, on the opposite side from the signal cards. This results in double ended termination, and allows all 13 slots to be used for signal cards. The RT value is 50 OHMS at each end of the backplane. VT is set to 1.5V with VREF (GTLP reference voltage) set to 1V. A simplified schematic for the backplane is illustrated in figure 11.

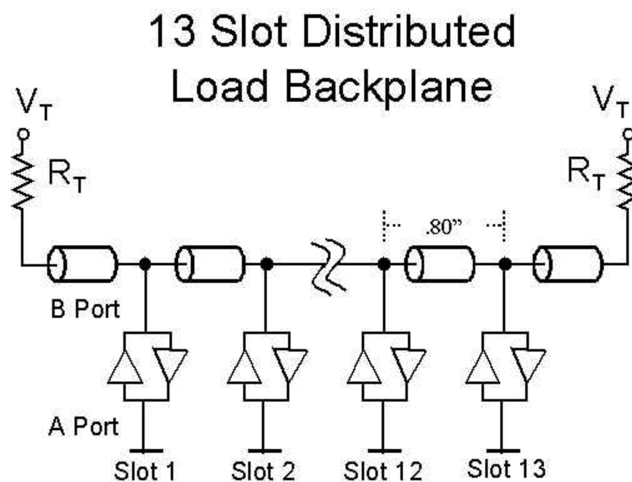


Figure 11 Simplified schematic of the 13 slot evaluation backplane

**Signal Evaluation**

Testing variables included loaded and unloaded backplane slots, and switching frequencies of 66MHz and 100Mhz. Test results show that although the GTLP in BGA and in TSSOP packages have roughly equivalent performance, there are notable differences in output wave shape.

Wave shape differences are seen on the output of the driver, the input of the receiver, and the output of the receiver. Less noise on the Voltage Output High ($V_{OH}$)and Voltage Output Low ($V_{OL}$) levels is present on the BGA packaged device, the BGA device also has slower output edge rates, in particular the falling edge.

In all evaluation waveforms shown, the top waveform is the TTL input, the 2nd waveform is the GTLP driver output, the 3rd waveform is the GTLP receiver input, and the bottom waveform is the TTL output.

66MHZ Loaded Backplane TSSOP and BGA Waveform Comparison

The waveforms for the comparison in Figures 12 and 13 are taken with the 13 slot backplane fully loaded (One driver card, 11 load cards, and one receiver card). The driver is placed in slot 1, and the monitored receiver is in slot 13, slots 2 through 12 each contain a load card. The driver has 4 outputs switching, and the frequency is set to 66MHz.

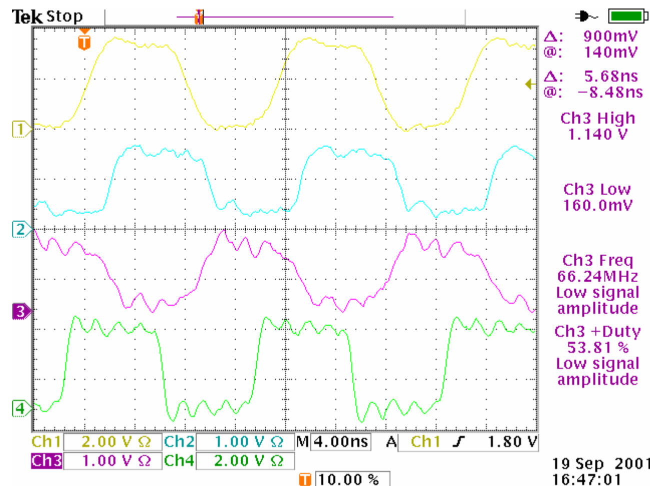


Figure 12 GTLP18T612 in 56 pin TSSOP at 66MHz

Noise is present on the $V_{OL}$ and $V_{OH}$ levels of the Driver output. Noise is also present at the receiver input and also on the TTL signal output.

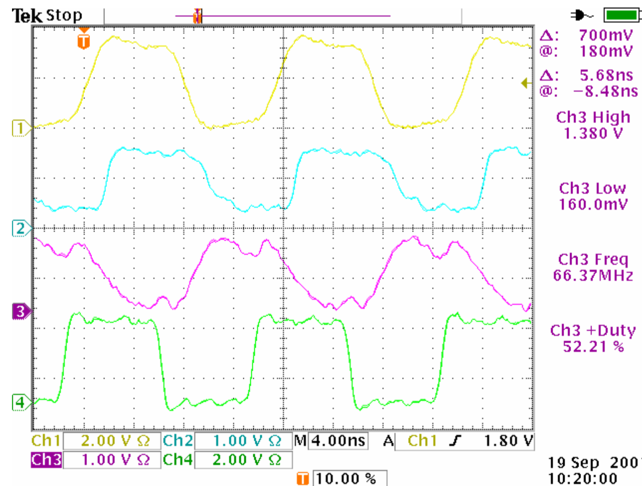


Figure 13 GTLP36T612 in 114 Ball BGA GTLP36T612 at 66MHz

The noise on the driver output $V_{OL}$ and $V_{OH}$ levels is significantly damped in comparison to the TSSOP driver output, the noise ripples present are of lower frequency and amplitude. The noise present at the receiver input and on the TTL output signal is of lower frequency and amplitude. The driver output edge rate is also slower, particularly the falling edge.

100MHZ Unloaded Backplane TSSOP and BGA Waveform Comparison

The waveforms for the comparison in Figures 14 and 15 are taken with the 13 slot backplane unloaded except for the driver and receiver cards. The driver is in slot 1, and the receiver in slot 13, all other slots are empty. The driver has 4 outputs switching, and the frequency is set to 100MHz.

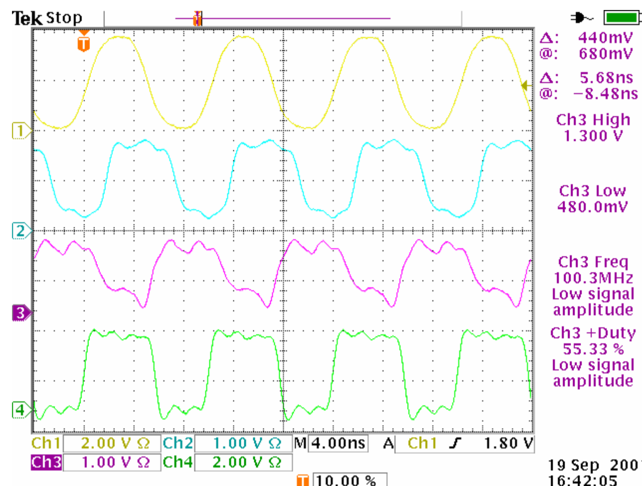


Figure 14 GTLP18T612 in 56 pin TSSOP at 100MHz unloaded

The output noise amplitude has decreased on the $V_{OH}$ level, and increased on the $V_{OL}$ of the Driver output, compared to 66MHz.

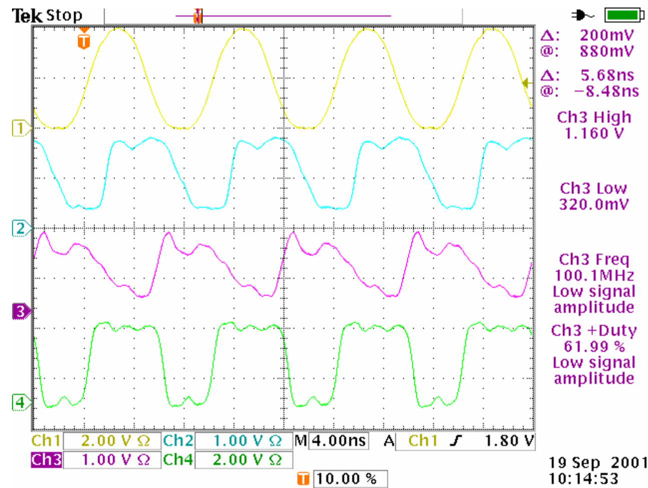


Figure 15 GTLP36T612 in 114 Ball BGA at 100MHz unloaded

The noise present on the driver output $V_{OH}$ is of lower frequency than on the TSSOP. The noise amplitude is about the same on the $V_{OH}$, and negligible on the $V_{OL}$. The driver output rising edge rate is about the same as the TSSOP, the falling edge is slower. Less noise is present on the TTL output signal.

## 100MHZ Loaded Backplane TSSOP and BGA Waveform Comparison

The waveforms for the comparison in Figures 16 and 17 are taken with the 13 slot backplane fully loaded (One driver card, 11 load cards, and one receiver card). The driver is placed in slot 1, and the monitored receiver is in slot 13, slots 2 through 12 each contain a load card. The driver has 4 outputs switching, and the frequency is set to 100MHz.

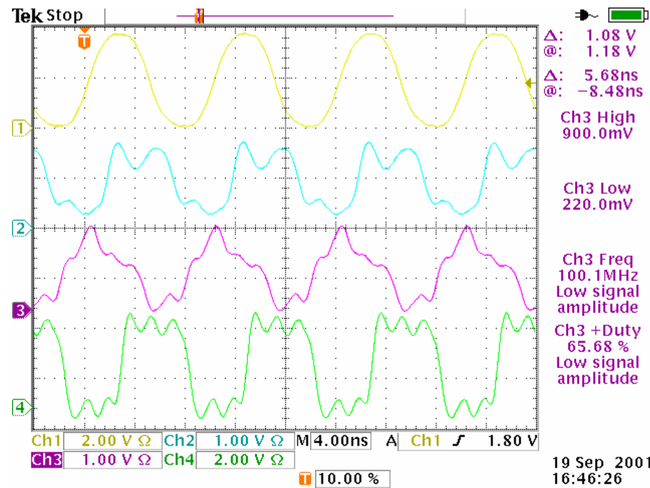


Figure 16 GTLP18T612 in 56 pin TSSOP at 100MHz loaded

The noise amplitude has increased on both the $V_{OH}$ level, and the $V_{OL}$ of the driver output, and has increased on the receiver output $V_{OH}$ and $V_{OL}$ levels, compared to the unloaded backplane at 100MHz . A $V_{OH}$ overshoot discontinuity is present at the receiver input.

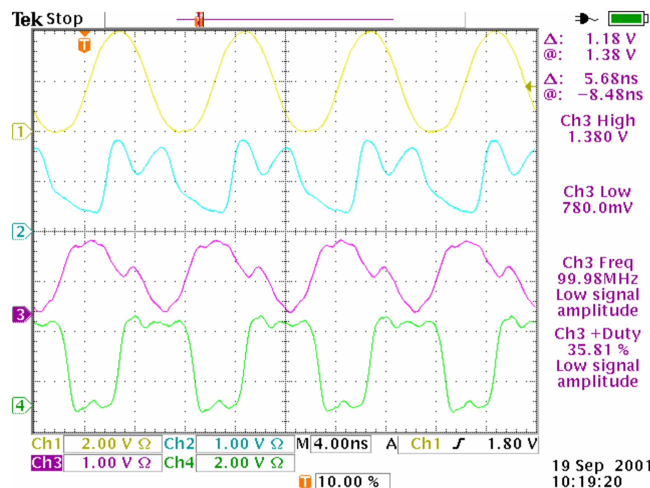


Figure 17 GTLP36T612 in 114 Ball BGA at 100MHz loaded

The noise present on the driver output $V_{OH}$ is the same frequency as the TSSOP, the amplitude is slightly higher (~100mV). Virtually no noise is seen on the $V_{OL}$. The driver output rising edge rate is about the same as the TSSOP, the falling edge is slower. Less noise is seen at the receiver input and less noise is seen on the TTL output signal.

## Edge rates

The BGA packaged GTLP device rising edge rates are as slow or slower than the TSSOP packaged devices across backplane loads and number of outputs switching. The BGA falling edge is consistently slower than the TSSOP falling edge rate. As the number of load cards or the number of outputs switching simultaneously increases, the signal rising edge for the two package types starts to achieve parity. Table 1 lists various configurations tested, and the resulting driver edge rates. The (# of cards) is the total number of cards connected to the backplane (i.e.: a 2 denotes the driver card and the receiver card only).

| Package | # of cards | # outputs switching | Frequency | Edge Rate |
|---|---|---|---|---|
| BGA | 2 | 4 | 33MHz | 5ns |
| TSSOP | 2 | 4 | 33MHz | 3ns |
| BGA | 13 | 4 | 33MHz | 5ns |
| TSSOP | 13 | 4 | 33MHz | 5ns |
| BGA | 2 | 32 | 33MHz | 6ns |
| TSSOP | 2 | 18 | 33MHz | 5ns |
| BGA | 13 | 32 | 33MHz | 5ns |
| TSSOP | 13 | 18 | 33MHz | 5ns |
| BGA | 2 | 4 | 66MHz | 2.6ns |
| TSSOP | 2 | 4 | 66MHz | 2.8ns |
| BGA | 13 | 4 | 66MHz | 2.4ns |
| TSSOP | 13 | 4 | 66MHz | 2.4ns |
| BGA | 2 | 32 | 100MHz | 3.2ns |
| TSSOP | 2 | 18 | 100MHz | 1.6ns |
| BGA | 13 | 32 | 100MHz | 2ns |
| TSSOP | 13 | 18 | 100MHz | 2ns |

Table 2 Comparison of BGA to TSSOP driver output edge rates.

Duty cycle

Both package types displayed a greater than 50% duty cycle for VOH. In many systems this is a benefit since the switching takes place on the rising edge. Slower rise times and more time at VOH increases the set and hold windows.

Skew and Propagation Delay

For this test, the backplane was configured with a driver card in slot 1 and a receiver card in slot 13. With one driver input switching 0V to 3V, and VREF set to 1.5V. Measurements were taken for the Low to High transition at the driver outputs. Skew was measured between the 2 internal die of the BGA, and 2 TSSOP packaged devices.

| Package | Device Pin | Delay |
|---|---|---|
| BGA 1 die 2 | 2B4 | 1.963ns |
| BGA 1 die 1 | 1B16 | 1.863ns |
| TSSOP 1 | B15 | 1.562nS |
| TSSOP 2 | B7 | 1.463nS |

Table 3 Comparison of BGA to TSSOP driver output skew.

The difference in delay numbers between the BGA and TSSOP devices is due in part to the location of the test points. Measurements for the TSSOP devices were taken at the leads. The BGA device measurements were taken at board test points and included 37ps of trace delay. The skew results are 100ps for the BGA, and 99ps between the 2 TSSOP packages. Propagation through the BGA device also takes approximately 400 ps longer than the propagation through the TSSOP device. Table 2 lists the results of the test.

The most significant performance difference between the two package types is the wave shape. The oscilloscope plots show that the BGA package filters out noise on the $V_{OL}$ and $V_{OH}$ of the signal more effectively than the TSSOP package. Edge rates and propagation delay also are different. The waveform evaluation illustrates that the BGA package for this device provides better noise margin by virtue of lower noise

amplitude on the waveform. In addition, as the load and frequency increased, the noise amplitude increased, the TSSOP would become unusable before the BGA due to excessive noise.

## Device and Package Modeling

Software for modeling device performance has been available for many years. There are many model options available to simulate an IC device, its packaging, and the circuit. Modeling software types include Cadence, H-SPICE, P-SPICE and IBIS. Commodity semiconductor manufacturers ordinarily supply device models to customers in H-SPICE and IBIS formats, as these are the model types typically requested by customers.

The modeling options and precision of the models and the software has been steadily improving. To accurately mimic packaging effects on IC signal performance, a model must contain an electrically precise example of the IC device and package. Furthermore, for simulations outputs to correctly represent all behavior nuances of the packaged device in the circuit, a full device model and accurate circuit parameters must also be used.

Frequently, the device and package models supplied by vendors are simplified Input Output sections of the IC. This type of simplified model is referred to as a 'slice' and generally the package portions of the model are also simplified. The benefits of using a slice include smaller model size for easier downloading, and a significant reduction in simulation run time. For a high degree of signal and performance accuracy, these models may not provide all the subtle waveform shape differences between package types. For example: a model of a 8 bit wide buffer that is simulating a slice of only one I/O path will not show between output capacitive coupling effects.

Semiconductor vendors are aware that faster edge rates yield a corresponding increase in package effects on device performance. Package modeling techniques and methods are advancing rapidly, and have become very sophisticated in this realm, with the goal of providing IC device designers with accurate information as to how the IC will perform in various package designs. This can help reduce performance differences by optimizing IC device and package combinations. Additionally, this knowledge is being used to develop customer models that are more advanced. The result is more accurate replication of IC and package combinations over all conditions.

## Conclusion

The effects of IC package on system performance have a direct effect on device performance and by extension system performance. These performance influences are related primarily to wave shape. Package effects include ground bounce and threshold effects, edge rate, skew, and propagation delay. Faster edge rates and higher frequencies make package differences more pronounced.

Most newer package designs offer improvements in signal performance. In some cases, these improvements can be significant. Some of these signal improvements are due to intentional design innovations, others are primarily side effects of package enhancements such as reduction in package size. However, it can not be taken as an absolute that a newer or smaller package will automatically offer improvements in signal performance. Nor can it be assumed that two externally identical packages from different vendors will offer equivalent performance.

By understanding how packages effect device performance, a system designer is better equipped to create a system that meets the performance requirements. As system speeds increase, changes in device packaging

must be considered with the same care as changes in board layout. In today's high speed systems, knowledge of the impact of package on IC device performance is imperative.

## *References*

Newberry W. Staff Design Engineer, Fairchild Semiconductor Corporation, Automation Development

Manzione, L.T., AT&T Plastic Packaging of Microelectronic Devices, Van Nostrand Reinhold 1990

Lau, J. H., Ball Grid Array Technology, McGraw Hill, 1995

Prasad, R. P., Surface Mount Technology, Chapman & Hall, 1989

Harper, C. A., Electronic Packaging and Interconnection Handbook, McGraw Hill, 2000