AN-139

PCB Design Considerations for KSZ8841/42 Family of Ethernet Controllers

Introduction

Successful high speed printed circuit board (PCB) design relies on carefully meeting system timing requirements as well as good board layout and decoupling in order to meet signal integrity concerns.

This application note gives some general guidelines and recommendations to facilitate the design of a robust PCB and reduce system debug time for KSZ8841/42 family of Ethernet controllers in LAN applications. The following topics will be discussed:

- PCB layout and layer strategy
- Power supply considerations and decoupling
- Ethernet front end design and ESD protection concerns
- Signal integrity issues
- Hands-on debug techniques for KSZ8841/42 board

PCB Layout and Layer Strategy

Micrel strongly recommends using at least 4-layer PCB for all high speed Ethernet LAN design since the printed circuit board cost is proportional to the number of layers, and to the board surface area. A typical 4-layer PCB stack-up uses high-speed differential and critical signal traces without vias to connect chips located on the top (component side) layer. The second layer is a solid and contiguous ground plane, with a solid power plane layer on layer 3, and a bottom signal traces layer on layer 4. The 4 layers partition and ground layer are shown in Figure 1.

PCB Design Consideration Notes:

1. Use a single ground plane approach with chassis ground plane (all layers) separated from the digital ground plane to reduce EMI as well as to improve the ESD protection, as shown in Figure 1.
2. Void both power and ground planes on all layers directly under the magnetics.
3. Do not route traces with 90-deg turns. Instead, use 45-deg turns and PCB trace widths should be designed to handle the amount of current that are expected.
4. Avoid vias and pads in the path on any critical signal since they will induce unwanted capacitance and inductance which can cause reflection and distortion due to a transient impedance discontinuity to a trace.
5. Make sure to have controlled impedances on all high speed signal traces with the correct termination schemes.
6. All high speed data/clock lines or differential traces should be of equal length.
7. Separate different clock domains between analog and digital circuitry components in order to avoid interference with each other.
8. Understand that the propagation delay for a microstrip (trace routed on an outer layer) is 145pS per inch while the stripline propagation delay (trace embedded between planes) is 180pS per inch.
9. Due to the material dielectric constant and power dissipation factor, FR-4 material is good for frequencies up to 500MHz and GE-Tek material can achieve up to 800MHz. GE-Tek materials offers performance enhancement over FR-4 with a price adder.
10. Position all crystal circuit components as close as possible to the input/output pins of device on the top layer and maintain a frequency tolerance within ±50PPM.

All datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

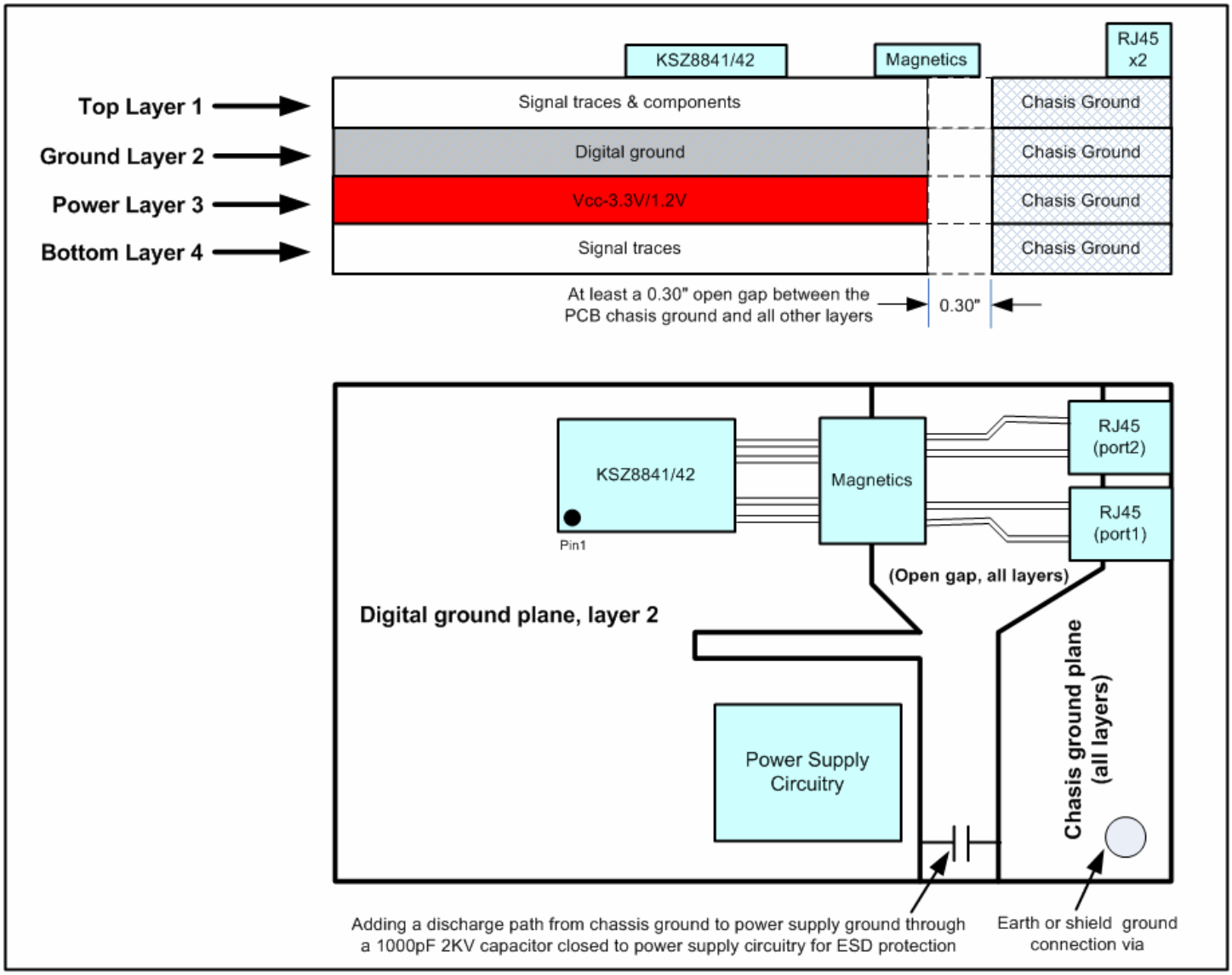

Figure 1. 4-Layer Partition and Group Plane Layout

Power Supply Considerations and Decoupling

Power supply and decoupling issues on printed circuit boards for high speed systems become more demanding as the performance is maximized. At the system level, high speed circuits generally consume more power than similar low speed circuits. This means that the power supply distribution system must be able to handle the larger current flow and the ground plane should cover as large an area as possible to reduce the length and inductance of the return path which can eliminate the ground noise. The best way to layout the circuitry on the printed circuit board is such that the highest speed device has the shortest signal leads, as well as the minimum return distances to the power supply and ground connections as shown in Figure 2.

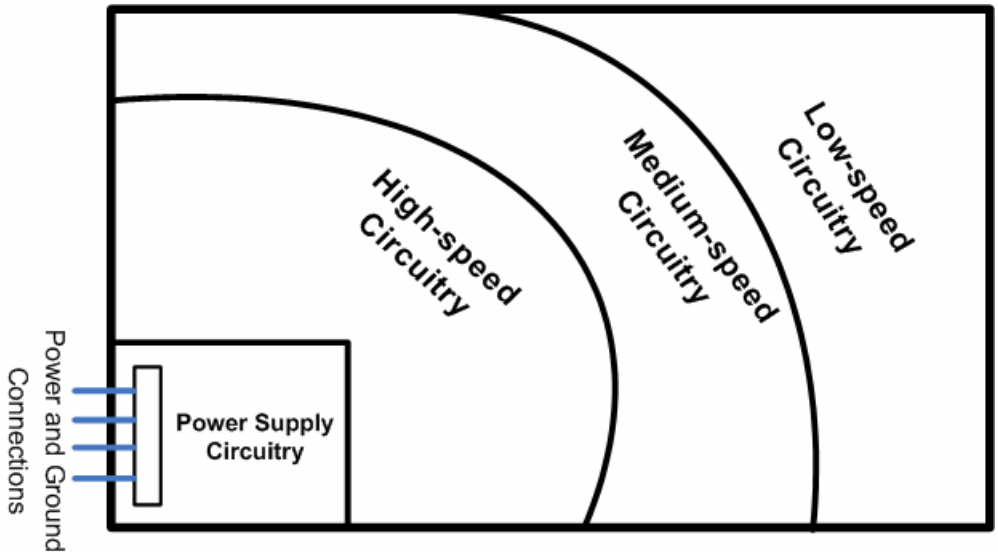

Figure 2. Segregation by Speed on Printed Circuit Board Layout

Decoupling Methods for KSZ8841/42

Generally speaking, the decoupling method can be divided into two stages on the board level design: power entry decoupling and chip level decoupling. With both methods, the decoupling capacitors and ferrite beads deliver a quick response and large burst of stable energy without generating a noise pulse and voltage droop in order to keep power and ground noise under 50mV peak-to-peak.

In a typical power distribution system design, the power entry capacitor is a relatively large-valued capacitor (100µF or larger) placed near the power entry point on the printed circuit board. The purpose of the power entry decoupling capacitor is to:

- Prevent transmission of PCB-generated noise to the backplane, motherboard and power supply.
- Supply power so that the voltage at the PCB power entry point is maintained at a stable level.
- Suppress power supply backplane ringing, resulting from inductance of the power supply and backplane.

In a high speed digital system design, the chip level decoupling capacitors (0.1µF or 0.01µF) and ferrite beads (at least 100Ω @ 100MHz) are primarily used to eliminate high speed transient switching noise and minimize troublesome high frequency clock harmonic components. Reducing the transient switching noise requires low inherent inductance within the decoupling capacitors and effective board design. When a capacitor is mounted on a board, the lead length and board trace (device V_{CC} to capacitor-to-ground) are a major source of inductance. This inductance must be minimized in order to obtain good decoupling performance under high speed transient conditions.

As shown in Figure 3, Micrel strongly recommends using a surface mount capacitor (SMD-0603 or smaller) to be placed as close as possible to power and ground pins to work best, and using a ferrite bead to isolate different V_{CC} power inputs. Ferrite beads are well suited for power supply filtering because they provide a series resistance at high frequency without causing a DC voltage drop. In this case, the series resistance is directly proportional to the frequency so that a ferrite bead allows low frequency signals to pass while attenuating high frequencies. Be sure to place bulk capacitors (10µF) on each side of the Ferrite bead.

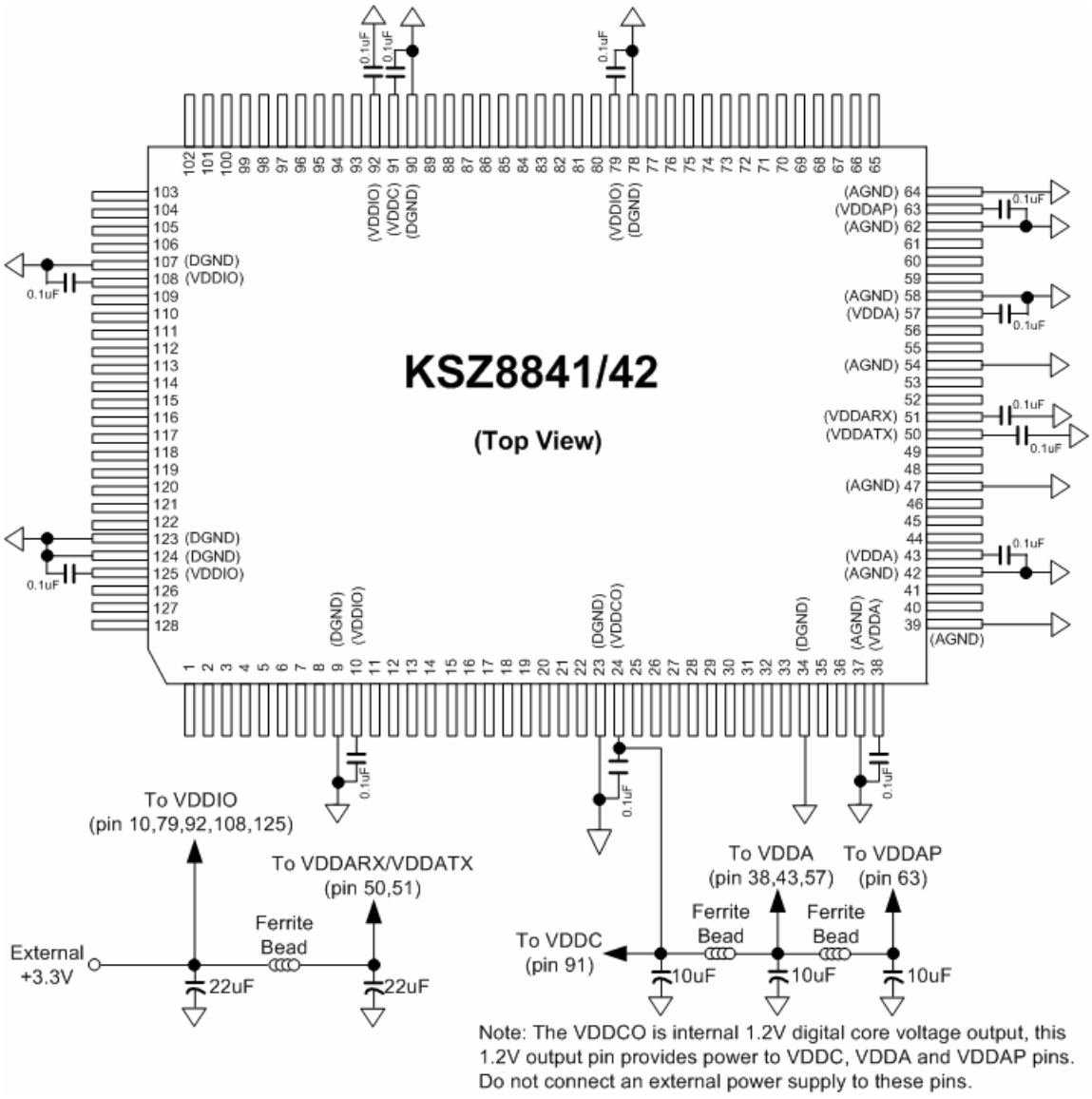

Figure 3. Decoupling and Power Supply Connections for Micrel's KSZ8841/42

Ethernet Front End Design and ESD Protection Concerns

The Ethernet front end schematic design for KSZ8841/42, as shown in the Figure 4, includes inter-connection details from RJ45 connector and transformer to the KSZ8841/42 devices.

Ethernet Front End Design Consideration Points to Remember:

1. The Transformer should be located as close as possible to the RJ45 connector.
2. The Transformer provides EMI and ESD isolation between KSZ8841/42 and RJ45 cable connection to the outside.
3. The KSZ8841/42 devices should be placed as close as possible to the Transformer.
4. In order to maximize ESD performance, the designer should consider choosing a discrete transformer without an integrated module of magnetic and RJ45. This can isolate between the Ethernet controller and the RJ45 connector to enhance the ESD performance.

5. Differential pairs (TX+/- or RX+/-) should be routed away from all of the other signals and close together, and should use 5-mil trace widths and 5-mil trace spaces of the same length and as short as possible, with a 100Ω controlled trace impedance pair.
6. Route TX+/- pair and RX+/- pair as far as away from each other with at least four times of 5-mil trace space.
7. If possible, keep all differential pair traces on the top component layer without using vias and referenced to the same power or ground plane layer.
8. The unused cable pairs on the RJ45 connector (pins 4&5, 7&8) should be terminated properly, as shown in Figure 4. These terminations should be routed with wide and short traces as close as possible to the RJ45 connectors.
9. A metal enclosed shield RJ45 connector is recommended and this shield should be connected directly to chassis ground to improve ESD protection.
10. Choose an RJ45 connector with surface mount contacts to simplify routing and without LEDs to enhance ESD performance.

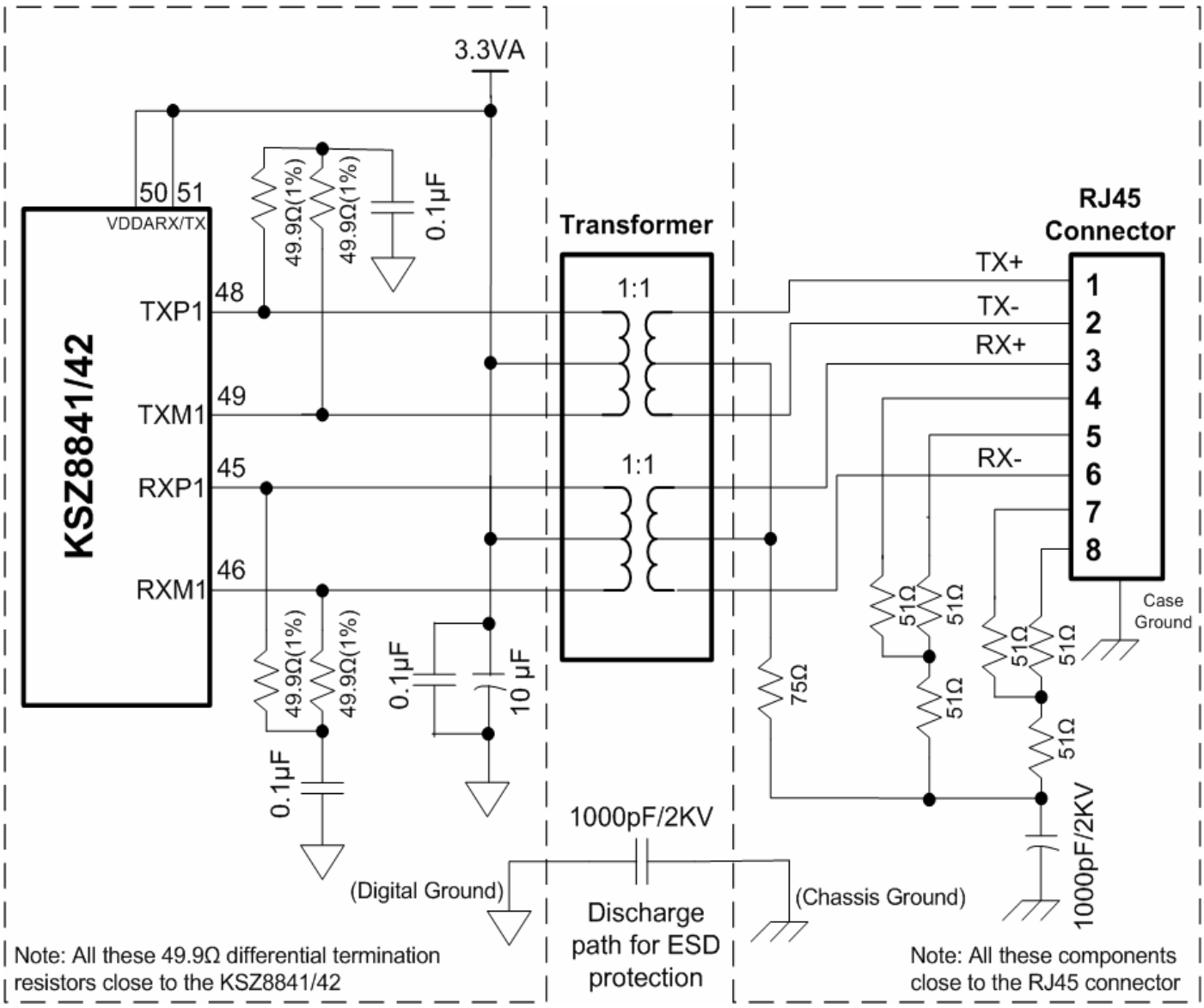

Figure 4. Inter-connection of Ethernet Front End for Micrel's KSZ8841/42 Port 1

ESD Protection Concerns

Electrostatic Discharge (ESD) costs the electronic industry millions of dollars annually in damaged or degraded parts, this kind of damage is the result of ESD energy shifting from one charged object to another object, so the electrostatic has become known as the silent killer.

What is ESD? Electrostatic Discharge (ESD) is a rapid current flow between two objects with different electrostatic potentials. ESD is a high-voltage transient with fast rise time and fast decay time. The damage associated with ESD in devices is primarily melting of the device material due to high temperatures, although sometimes with very rapid events, the damage mechanism can punch through the oxide layer due to high electrical field strengths. Typical sources of ESD stress type include Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM); the differences among these sources exist in their transient voltage (KV) and peak current (10s of amperes) levels.

Devices will normally experience an ESD event during normal handling and operating conditions. A typical and often used example is that of an operator gathering charge by walking across a carpet and then handling a device. As the operator touches the device (at high voltages a discharge can occur before physical contact), there is a rapid equalization of potentials between the operator and device. While very unlikely to happen in this way today with modern manufacturing environments and procedures, the example is still one that many of us have experienced.

Destructive discharges can be undetectable by a human operator since the energy levels involved are often very small and below human thresholds for detection. However, for a device these discharges can be and often are fatal. Although the energy may be low, the device must dissipate it as heat. Silicon is a very poor conductor and therefore small levels of energy delivered quickly can easily cause the material to melt and deform due to the silicon's inability to dissipate the heat fast enough. After the material has been deformed by a highly localized temperature, the device is permanently damaged. It is important to remember that not all ESD discharges are instantly fatal; many will only weaken the device making it less likely to provide reliable and long-term operation.

Preventing ESD can be easy and inexpensive. Two basic rules for static protection are as follows:

- Handle all static-sensitive devices at a static safeguarded work area.
- Transport all static-sensitive devices in static shielding containers or packages.

Eliminating electrostatic in the workplace is accomplished by grounding operators, components and equipment. Grounding prevents static charge buildup and electrostatic potential differences. Electrical field damage is averted by transporting products in special electrostatic shielding packages.

The most important issue for designing PCBs with ESD compliance is to carefully consider how the ESD currents will flow to earth and where the ESD voltages will appear, to avoid other circuitry malfunctioning or even being destroyed. The following ESD design guidelines for PCB should be considered:

- Place voltage-clamping devices such as transient voltage suppressor (TVS) on the TX+/- and RX+/- differential pairs to limit the surge voltage to a safe level for the circuit or component being protected.
- Terminate the unused pairs (pins 4, 5 & 7, 8) in the RJ45 cable connector with 51 ohms and connect them with a high voltage capacitor (2KV) to the chassis ground of the PCB. This chassis ground on the PCB is directly connected to the metal shield of the equipment, and this metal shield ground path continues through the power supply, power cord to earth ground so that any ESD high voltage entering on these unused pairs will pass to earth ground without damaging the circuit or the device.
- The active signal pairs (pins 1, 2 & 3, 6) in the RJ45 cable connector are connected to the transformer which has been rated for a high breakdown voltage. When the ESD energy enters the transformer and exits to the center taps of the transformer, these center taps are terminated with 75 ohms and connected to a high voltage capacitor (2KV) to the chassis ground of the PCB. The chassis ground on the PCB is directly connected to the metal shield of the equipment, and this metal shield ground path continues through the power supply, power cord to earth ground so that any ESD energy entering on these signal pairs will pass to earth ground without damaging the circuit or device.
- Add a discharge path from chassis ground to power supply ground through a 1000pF 2KV capacitor to allow the ESD energy flow to the supply ground first and then the device ground.

Due to the nature of ESD, it must be assumed that all devices will encounter an event during the normal course of their lifetime. Hence, ensuring that devices provide a reasonable and acceptable level of tolerance to ESD is an important part of all device design and manufacturing programs.

Signal Integrity Issues

The printed circuit board traces that carry high speed digital signals behave like transmission lines. The transmission line effects can cause reflection, ringing, distortion, and crosstalk between adjacent lines. Understanding this behavior is important for trouble-free board design. A basic rule of thumb is that printed circuit board traces should be treated as transmission lines if the unloaded signal transition (rise/fall) time at the driving end is equal or less than the round-trip propagation delay on the trace. Typically the transmission line delay is about 160pS per inch on the trace. For example, if a signal transition time is 1.0nS then a trace longer than 3.125 inches should be considered as a transmission line.

Printed circuit boards should be developed with transmission line impedance as constant and controlled as possible. A solid ground plane is required to establish controlled (known) impedance for the transmission line interconnections.

There are three mainly noise related problems with respect to the signal integrity:

- **Ringing/Reflection**

  Unbalanced (discontinuous) impedance, stubs, vias, interconnector and unmatched termination generally cause undesirable effects such as ringing or reflection in a circuit. For high-current switching, you must take great care to minimize the inductive/capacitive loading and cut ringing/reflection by providing better matching of the source and load impedances to the transmission line.

- **Crosstalk**

  Crosstalk is an undesirable electromagnetic coupling between signal traces and vias. The possibility for such signal coupling increases as the length along which the traces running in parallel increases. Faster switching also creates more crosstalk. Crosstalk can be attenuated by separating the adjacent traces as much as possible. Ground striping or shielding is another effective way to reduce crosstalk, and it makes better use of the available board area. Ground striping is a ground trace run between the two parallel traces. When it is feasible, the best way to minimize crosstalk is to route traces on separate layers of the board, with embedded ground or power traces between layers.

- **Ground Bounce**

It is also called power/ground noise due to parasitic inductances of the V_{CC}/Gnd delivery system during which all drivers simultaneously switch fast output signals. The shorter transition (rise) time has a higher di/dt which causes more ground bounce inside the chip package due to the lead inductances. Decoupling is an important aspect in power/ground noise such as optimized decoupling capacitors, placement, and the right combination of decoupling values which we have discussed in the previous section.

Hands-on Debug Techniques for the KSZ8841/42 Board

Micrel's KSZ8841 is a one-port and the KSZ8842 is a two-port Ethernet Controller. The host interface is designed for 8-, 16- or 32-bit bus interfaces. This subsection provides a basic board debugging checklist as shown below:

1. Check power supply for VDDIO-3.3V (pins 10, 79, 92, 108, 125) and VDDARX/TX-3.3VA (pins 50, 51). The center taps of transformer on the KSZ8841/42 device side need to connect 3.3VA.
2. Power supply 1.2V output from VDDCO (pin 24) is connected to VDDC (pin 91), VDDA (pins 38, 43, 57) and VDDAP (pin 63). This 1.2V core power supply is for internal logic only. Do not use this supply for other circuits or devices.
3. All ground pins (analog and digital) are connected to the same continuous ground plane.
4. Check the 25MHz clock at X1 input pin 65 and check that this clock requirement is within ±50ppm for either the crystal or the oscillator.
5. The reference voltage of ISET at pin 61 is 500mV and this pin is pulled-down with a 3.01K (1%) resistor to ground.
6. The default base address is 0x0300 when EEEN (pin 26) is pulled-down (without EEPROM). The EEDI (pin 30) can be pulled-down for the 8-bit bus mode and pulled-up for the 16-bit bus mode, or don't care for the 32-bit bus mode (for KSZ8841/42M non-PCI devices only).
7. The default base address is loaded from the external EEPROM when the EEEN (pin 26) is pulled-up (with EEPROM), EECS (pin 19) connects to EEPROM's CS pin, EESK (pin 29) connects to EEPROM's SK pin, EEDO (pin 28) connects to EEPROM's DI pin, and EEDI (pin 30) connects to the EEPROM's DO pin (for KSZ8841/42M non-PCI devices only).
8. An external 4.7K pulled-up resistor is required on following pins: ARDY (pin 20), INTRN (pin 16).

9. Measure the normal link pulse waveform on either TX+/- or RX+/- every 16ms while the cable is not connected, as shown in Figure 5.
10. Measure the normal 100BT frames transmitting/receiving waveform on either TX+/- or RX+/- when the cable is connected, as shown in Figure 6.
11. Check that there is a minimum of 1ns (t1 in the data sheet) while A[1:15], AEN, BExN[3:0] are valid when RDN, WRN are asserted in the host asynchronous interface (for KSZ8841/42M non-PCI devices only).
12. Check that there is a minimum of 1ns (t2 in the data sheet) hold time for A[1:15], AEN, BExN[3:0] after RDN, WRN are de-asserted in the host asynchronous interface (for KSZ8841/42M non-PCI devices only)

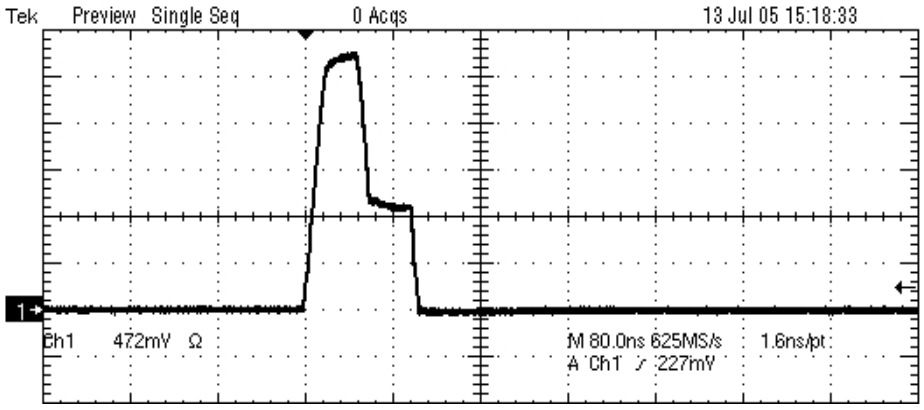

Figure 5. Link Pulse Timing Waveform (100nS and 1.5V p-p)

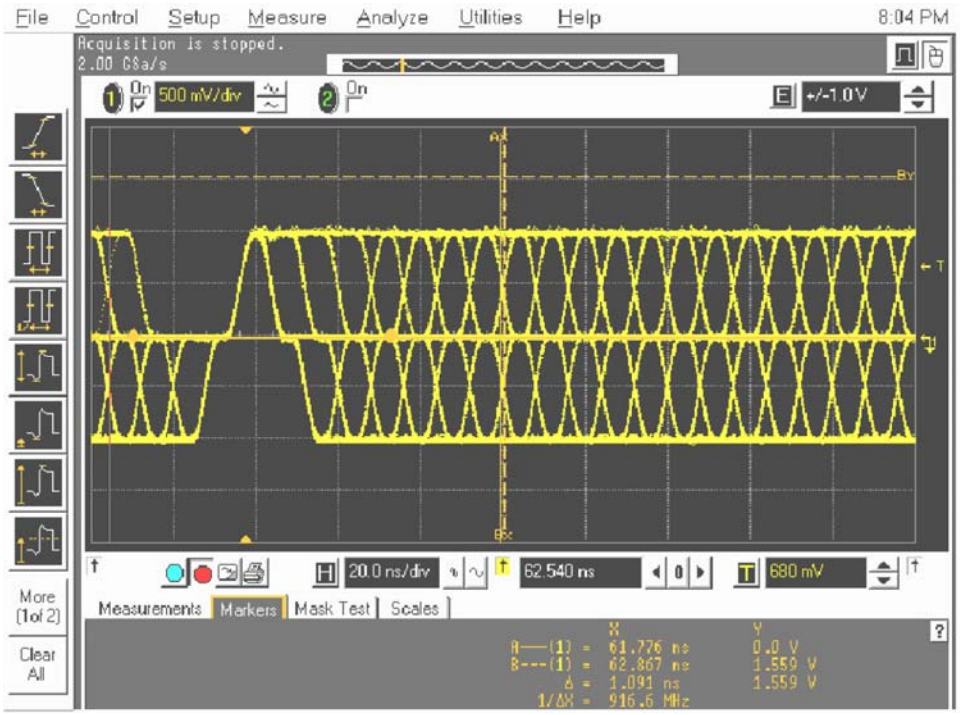

Figure 6. Normal 100BT Output Waveform

Conclusion

This application note has highlighted the important PCB design considerations of layout, power supply, decoupling and ESD protection, when using the KSZ8841 and KSZ8842 Embedded family of Ethernet Controllers.

Micrel has the largest family of single and dual ports Embedded Controllers in the industry today. All of the development collaterals including the data sheets, schematics, Gerber files, IBIS models and software drivers can be downloaded from Micrel's website. Evaluation boards and user's guide are also available.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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