

Bandwidth, OFF Isolation and Crosstalk Performance of the ADG5XXA Multiplexer Series

by Dan Sheehan and Matt Smith

The ADG5XXA* multiplexer series is a family of single 8/16 channel and dual 4/8 channel parts. They are available in both latched (ADG52XA) and unlatched (ADG50XA) versions. These are high performance multiplexers that offer the following notable features: specifications for both single and dual supply operation, 1 nA max leakage current, 200 ns max turn-on and turn-off times and TTL compatibility with reduced single or dual supplies down to 5 V.

Multiplexers are widely used on the front end of data acquisition systems where there is an ever increasing requirement for higher accuracy. This requirement, coupled with the availability of increased resolution A/D converters that are capable of digitizing higher frequency signals, has dramatically heightened the need for a good understanding of the ac performance characteristics of multiplexers. Also, to be able to apply the multiplexers in applications such as RF, radar and video switching, the ac performance characteristics must be understood. The ac parameters of interest in a multiplexer are its varying impedance characteristics versus frequency and are principally bandwidth, off isolation and crosstalk.

Although the multiplexers of the ADG5XXA series are low cost, general purpose parts, their ability to switch high frequency signals is excellent. The parts are fabricated in Linear Compatible CMOS (LC²MOS), an advanced process that features very low parasitic capacitances and, consequently, improved bandwidth, off isolation and crosstalk performance.

This application note investigates the bandwidth, off isolation and crosstalk of the ADG5XXA series from a practical engineering viewpoint by presenting typical application circuits with results, over the dc to 20 MHz frequency range. The emphasis is very much on practicalities and so the results are stated rather than derived, though it is intended that the reader will gain some insight into the mechanisms which affect the high frequency performance of the multiplexers.

*ADG506A/ADG507A, ADG508A/ADG509A, ADG526A/ADG527A, ADG528A/ADG529A.

MULTIPLEXER EQUIVALENT CIRCUIT

A simplified ac equivalent circuit for a pair of adjacent switches in a multiplexer is shown in Figure 1. For high frequency applications it is essential that the parasitic elements shown in the model are taken into account.

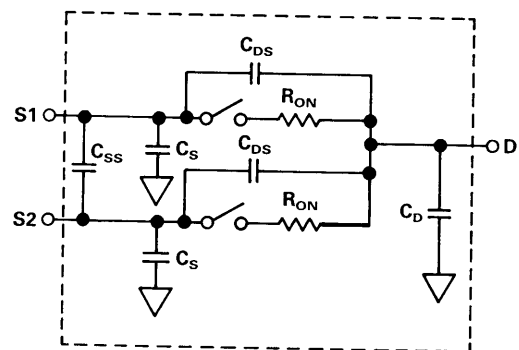


Figure 1. Equivalent Circuit for Adjacent Switches

Element	Title
C_{DS}	Drain-Source Capacitance
C_S	Source Capacitance to GND
C_D	Drain Capacitance to GND
C_{SS}	Capacitance Between Sources
R_{ON}	Channel ON Resistance

Table 1. Parasitic Elements

The equivalent circuit simplifies further depending on which switch parameter (bandwidth, crosstalk or isolation) we are concerned with. These parameters will now be discussed separately.

BANDWIDTH

The 3 dB bandwidth frequency provides a measure of the high frequency usefulness of the ADG5XXA series in the ON state.

From an ac or bandwidth perspective, the ON state equivalent circuit of a multiplexer channel can be simplified to a series resistance and shunt capacitance model, as shown in Figure 2.

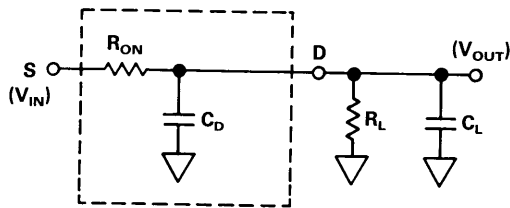


Figure 2. ON Channel Equivalent Circuit

The transfer function (V_{OUT}/V_{IN}) for the ON channel is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{R_L}{R_L + R_{ON}}}{1 + j2\pi f \left[\frac{R_L \cdot R_{ON}}{R_L + R_{ON}} \right] [C_D + C_L]} \quad (1)$$

The 3 dB break frequency f_o , is:

$$f_o = \frac{1}{2\pi \left[\frac{R_L \times R_{ON}}{R_L + R_{ON}} \right] [C_D + C_L]} \quad (2)$$

Therefore, for dc or low signal frequencies ($<f_o$), the multiplexer channel functions as a simple resistive conduction path ($R_{ON} = 180 \Omega$ typ for all parts), and any ON insertion loss (attenuation of V_{IN}) is limited to the ratio of $R_L/(R_{ON}+R_L)$. It is with higher signal frequencies that the complex ac impedance shown in Figure 1 becomes significant, resulting in additional attenuation of the analog input signal.

From Equation 2 it is clear that the bandwidth is limited by R_{ON} , R_L , C_L and C_D . Normally $R_L \gg R_{ON}$ in order to minimize the insertion loss, so the bandwidth is limited mainly by R_{ON} , C_D and C_L . The ADG5XXA series of multiplexers exhibit extremely low parasitic drain capacitance C_D . To take advantage of this low C_D , the external load capacitance should be kept as low as possible. Stray capacitance at the MUX output contributes to C_L , so it is important that this be minimized by proper circuit board layout with signal line lengths as short as possible. Bandwidths in excess of 40 MHz may be achieved with reasonable care. The ON resistance R_{ON} may be minimized by operating with ± 15 V power supplies and low input signal levels. (See ADG5XXA data sheets for further information on R_{ON} variation.) The frequency response roll-off rate is typically 20 dB/decade, i.e., single pole roll-off rate.

Figure 3 shows the test circuit used to evaluate the bandwidth performance of the ADG508A. Similar type test circuits apply for the other parts also.

Figure 4 shows a plot of bandwidth vs. load capacitance for the ADG508A and ADG528A. The same results apply for all the input channels and over all package types. From the plots it can be seen that C_L is critical to the bandwidth performance. Nevertheless, 12 pF yields excellent results, with $f_o > 40$ MHz.

Similar results would apply for the ADG509A and ADG529A, but the break frequency (f_o) would be slightly higher due to the even lower C_D of these parts.

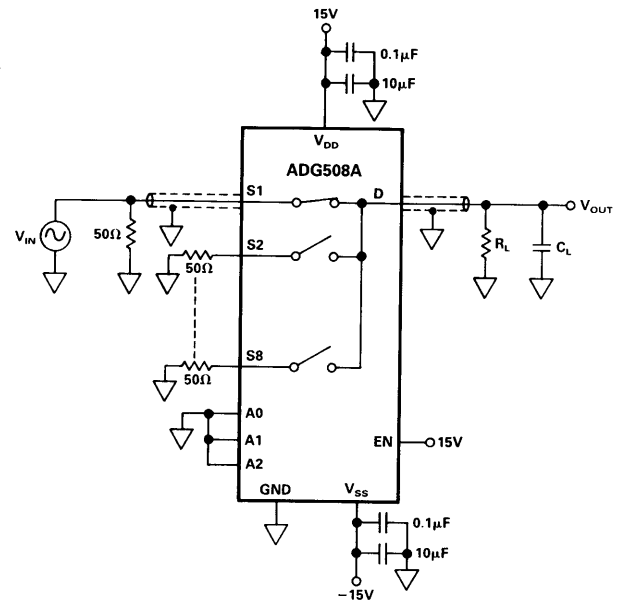


Figure 3. ADG508A Bandwidth Test Circuit

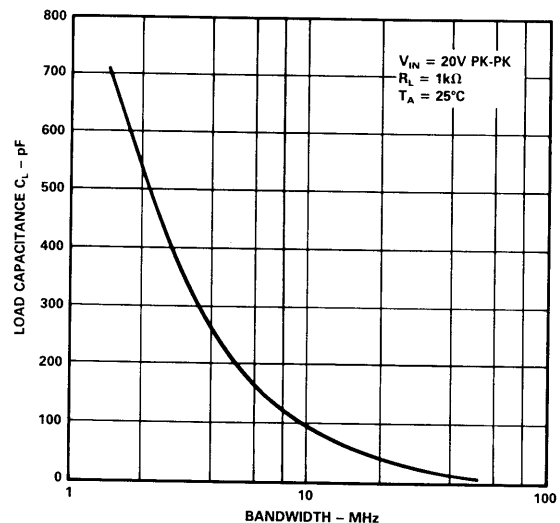


Figure 4. ADG508A and ADG528A Bandwidth Results

The 3 dB break frequency of the ADG506A and ADG526A, with an R_L and C_L of 1 k Ω and 12 pF respectively, is typically 30 MHz. Again, similar results apply for the ADG507A and ADG527A, but with a slightly higher f_o .

OFF ISOLATION

Although the bandwidth performance (ON state) is very important, most applications involving the switching of high frequency signals are frequency limited due to reduced OFF isolation rather than degraded ON performance. OFF isolation is a measure of the ability of the multiplexer to block ac signals in the OFF state and is defined by the following equation:

$$\text{OFF Isolation}^*(\text{dB}) = 20 \log (V_{IN}/V_{OUT}).$$

*Due to popular convention, OFF isolation and (crosstalk) values are positive number.

From an OFF isolation point of view, the multiplexer channel (or switch) can be modelled by the circuit shown in Figure 5. C_{EQ} , which allows signal coupling from the source (S) to the drain (D), determines the OFF impedance presented by the multiplexer to ac signals. Therefore, as the signal frequency increases, C_{EQ} passes more signal to the output. C_{EQ} is a combination of the OFF state parasitic capacitance of the relevant multiplexer channel and external stray capacitances due to wiring and circuit board layout.

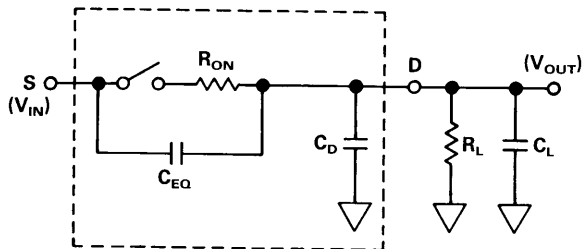


Figure 5. OFF Channel Equivalent Circuit

The OFF state parasitic capacitance of the multiplexer channel depends on a number of factors. These factors are principally: fabrication process (LC²MOS), pin configuration and package type (plastic DIP, Cerdip, PLCC). It has already been noted that the LC²MOS process features very low parasitic capacitances. The optimum pin configuration minimizes the parasitic capacitance by keeping the the analog input and output pins as far apart as possible. The effect of pin configuration and package type is highlighted in the results.

Minimizing the stray capacitance, to achieve lower values of C_{EQ} , is critical in achieving the optimum OFF isolation specifications. Coaxial cable should be used to transmit the analog signals and a good circuit board layout is vital. The circuit board should use short signal tracks with guard traces between them, ground planes and bypassed power supplies.

In addition to C_{EQ} , the OFF isolation is also determined to a large degree by C_D , C_L and R_L . The lower the value of R_L , the better the OFF isolation performance (C_{EQ} 's reactance becomes less effective), but note, a low value of R_L gives increased on-insertion loss (i.e., ratio of $R_L / [R_{ON} + R_L]$). Obviously, the choice of the R_L value involves tradeoffs to suit a particular application. Large values of C_D and C_L improve the OFF isolation performance but again this leads to reduced bandwidth in the ON state.

The results which follow apply for an optimized circuit board layout and illustrate how some of the factors outlined above influence the OFF isolation performance. A careless circuit board layout will give degraded results. Figure 6 shows one of the test circuits used to measure the OFF Isolation of the ADG508A (similar test circuits for the other parts).

ADG508A Series* Results

Typical OFF Isolation plots for the ADG508A and ADG528A are shown in Figures 7, 8, 9 and 10.

*ADG508A/509A, ADG528A/529A.

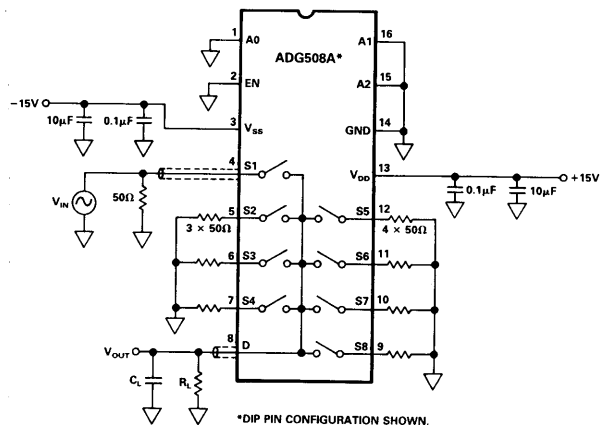


Figure 6. ADG508A OFF Isolation Test Circuit

The slope of most of the OFF isolation plots changes versus frequency, and this is very apparent from Figure 10 for different values of R_L . At low frequencies the fall off rate is typically 20 dB per decade. However, the OFF channel equivalent circuit has a pole frequency at $f_p = 1/2 \pi (C_{EQ} + C_L + C_D) R_L$. Therefore, as the signal frequency approaches and then becomes greater than the pole frequency, the fall off rate decreases and flattens out.

The OFF isolation performance varies with package type due to the different lead frames used. Overall, the plastic leaded chip carrier (PLCC) gives the best results, followed by the plastic DIP and then the cerdip. The PLCC performs best because it has the smallest lead frame, giving the least parasitic capacitance between the input and output pins.

For both the plastic DIP and PLCC packages (No Connect pins are grounded), the input channel with the worst case OFF isolation is S4 (adjacent the output, D), followed by S3 with the best performance from S1 and S5 (same results). For the cerdip package, the worst case channel is again S4, but it is followed closely by S8 and then S3, with the best results from S1 and S5. The difference between this package and the plastic DIP is due to a different lead frame configuration. The plots also show the OFF isolation performance for all the input channels (S1 to S8) driven simultaneously.

From the plots for the ADG508AKN (see Figure 8), it can be seen that S4 couples more unwanted signal into the output than the remaining seven channels put together. Therefore, by sacrificing the use of Channel 4, the user can obtain excellent OFF isolation results from the remaining seven channels. Alternatively, to achieve even higher isolation from the seven channels, S4 may be utilized as a NORMALLY ON grounded channel. With this scheme, S4 is selected when all the other channels are off. This effectively grounds the output (via R_{ON}) giving improved OFF isolation results which are independent of R_L . Hence large values of R_L may be selected which minimize the ON insertion loss without degrading the isolation. The improvement offered with this scheme is included in Figure 10.

Similar results apply for the ADG509A and ADG529A, except at high frequencies where the OFF Isolation is marginally worse due to the lower C_D of these parts.

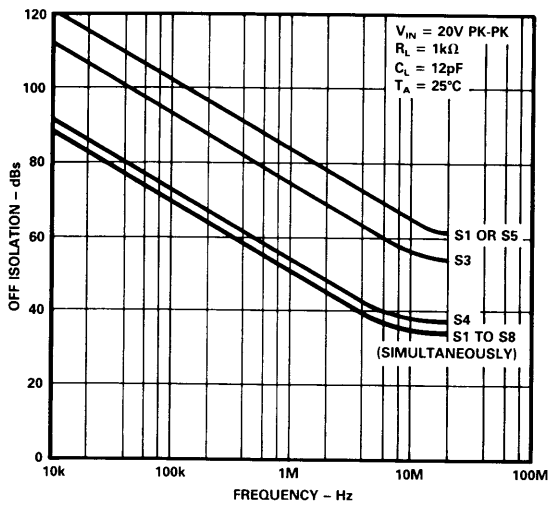


Figure 7. ADG508AKP and ADG528AKP (PLCCs) OFF Isolation vs. Frequency

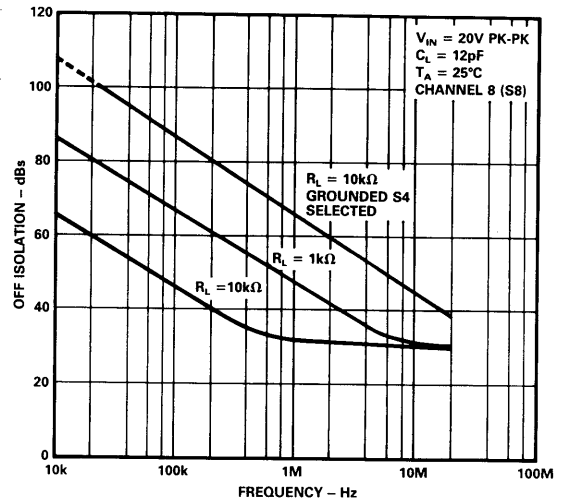


Figure 10. ADG508ABQ and ADG528ABQ (Cerdips) OFF Isolation vs. Frequency for Different R_L

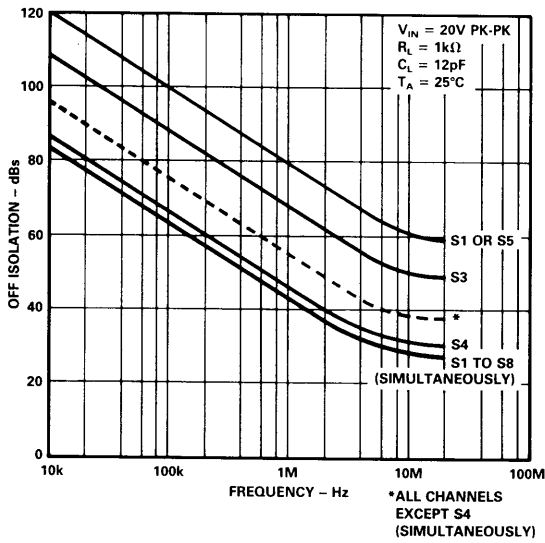


Figure 8. ADG508AKN and ADG528AKN (Plastic DIPs) OFF Isolation vs. Frequency

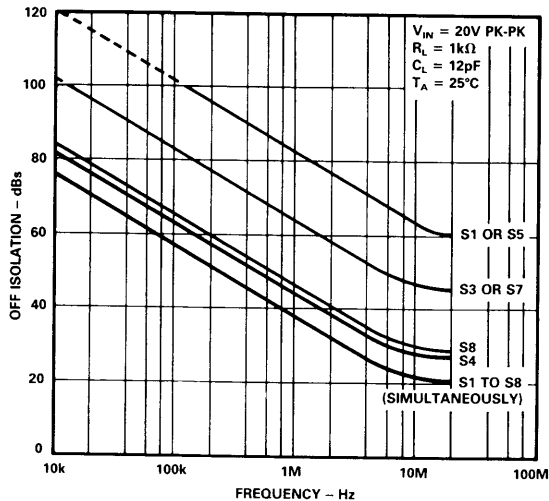


Figure 9. ADG508ABQ and ADG528ABQ (Cerdips) OFF Isolation vs. Frequency

ADG506A* Series Results

Typical OFF isolation plots for the ADG506A and ADG526A are shown in Figures 11 and 12. The ADG507A and ADG527A would yield similar results except at the high frequency end where the results would be marginally worse due to the lower C_D of these parts.

Since the ADG506A series has no analog input channel on a pin which is adjacent to the output, the results for this series surpass those for the ADG508A series. For both the DIP and PLCC packages (N.C. pins connected to GND), the input channel with the worst case OFF isolation is S8, followed by S7, with the best performance from S1 and S9.

In general, comments concerning the ADG508A series results apply for the ADG506A series also.

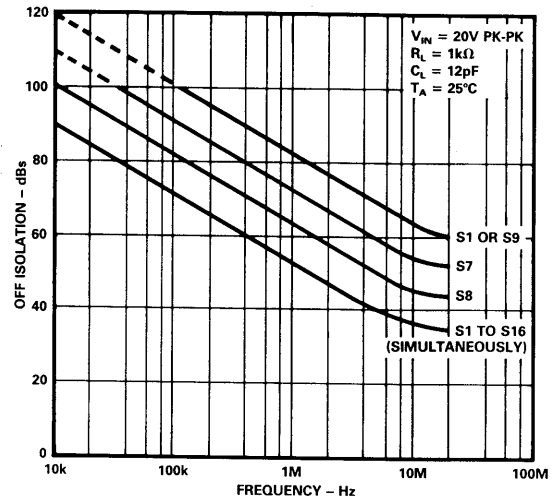


Figure 11. ADG506AKN and ADG526AKN (Plastic DIPs) OFF Isolation vs. Frequency

*ADG506A/507A, ADG526A/527A.

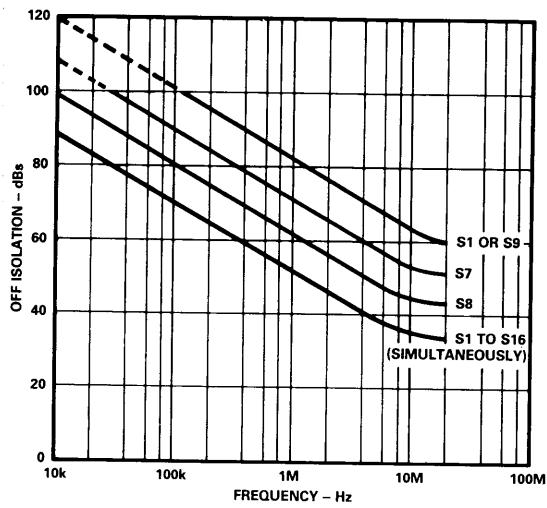


Figure 12. ADG506ABQ and ADG526ABQ (Cerdips) OFF Isolation vs. Frequency

CROSSTALK

Crosstalk, which is also called Channel-to-Channel Crosstalk, is another frequency-dependent factor. It is basically channel-to-channel isolation and occurs due to the OFF state parasitic capacitances of the multiplexer. Figure 13 shows a simple crosstalk model for a two-channel multiplexer. Assuming negligible ON insertion

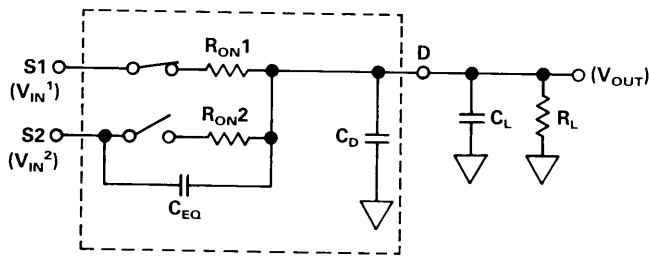


Figure 13. Crosstalk Equivalent Circuit

loss due to R_{ON1} and R_L , V_{OUT} should equal V_{IN1} . However, C_{EQ} (see OFF isolation section for details) couples some portion of V_{IN2} into V_{OUT} . Also, but to a lesser degree, additional signal coupling (not shown in Figure 13) occurs between the switches due to parasitic capacitances within the die and between the package leads. With V_{IN1} connected to GND, crosstalk for the circuit shown in Figure 13 is defined by the following equation:

$$\text{Crosstalk (dBs)} = 20 \log (V_{IN2}/V_{OUT}).$$

The error signal couples into a parallel combination of R_L , R_{ON1} , C_D and C_L versus R_L , C_D and C_L only for OFF isolation. Because R_{ON} is typically 180Ω , crosstalk results are generally 10 dB better than OFF isolation results.

While maintaining good bandwidth and OFF isolation performance, crosstalk can be minimized by choosing a multiplexer with a low R_{ON} . A good circuit board layout that shields the analog signals and keeps stray capacitances to a minimum is also vital.

Figures 14 and 15 show two of the test circuits used to measure the crosstalk of the ADG508A (similar test circuits used for the other parts).

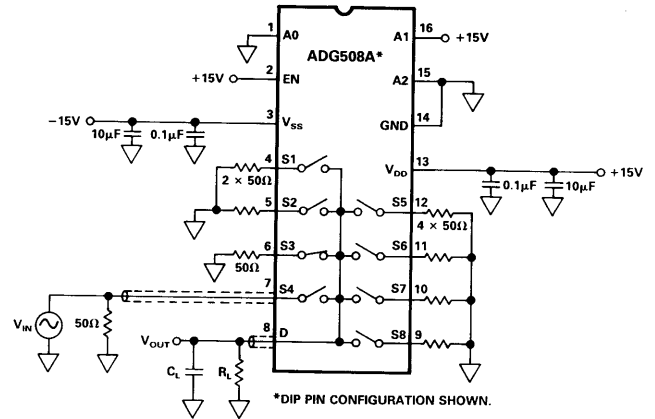


Figure 14. ADG508A Crosstalk Test Circuit (One OFF Channel Driven Only)

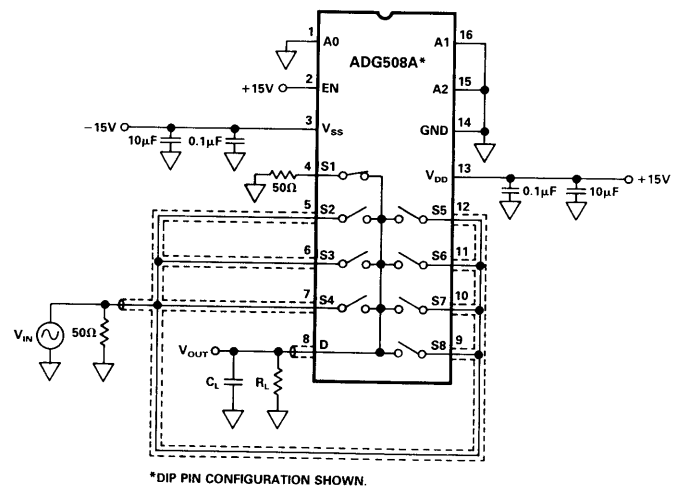


Figure 15. ADG508A Crosstalk Test Circuit (7 OFF Channels Driven)

ADG508A Series Results

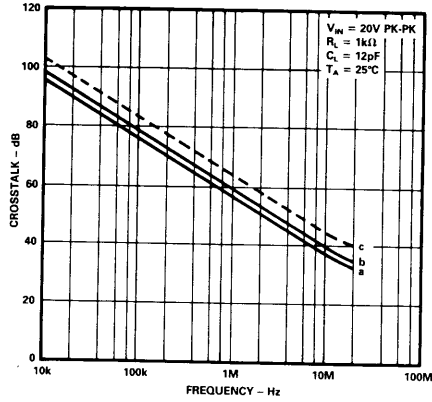
Typical crosstalk plots for the ADG508A and ADG528A are shown in Figures 16, 17 and 18.

In Figure 14, the crosstalk is measured by driving S4 only, with S3 selected and the remaining OFF channels connected to GND via 50Ω . Due to the proximity of S4 to the output pin, driving this channel gives the worst case crosstalk results (for one OFF channel driven only) – see Figure 16 Plot b. For example, driving S3 only with S4 selected would give far superior results – typically 15 dB better in the case of the ADG508AKN and ADG528AKN.

Crosstalk can also be measured by driving all of the remaining OFF channels simultaneously, with any one channel selected as in Figure 15. Under these conditions the worst case performance (see Figure 16 Plot a) occurs when S1 or S5 is selected and the best performance (see Plot c) results when S4 is selected.

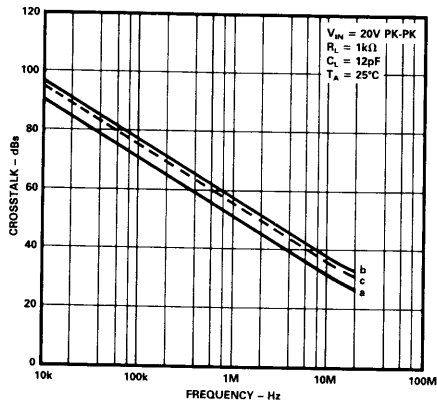
The plastic DIP package gives better results than the cerdip package (similar to OFF isolation). The results for PLCC are not shown but would be approximately 5 dB better than for plastic DIP. Figure 18 shows that the crosstalk performance improves as R_L reduces.

Similar results would apply for the ADG509A and ADG529A. However, at the high frequency end, the results would be marginally worse due to their lower C_D .



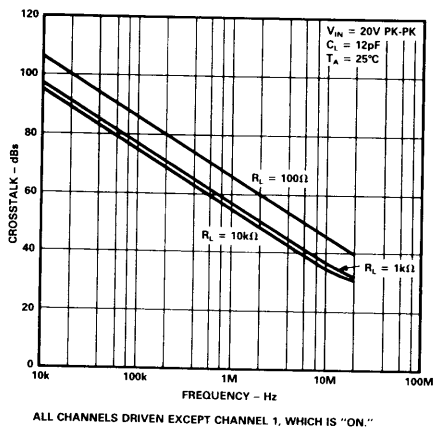
a. ALL CHANNELS DRIVEN EXCEPT CHANNEL 1, WHICH IS "ON."
 b. S4 DRIVEN; S3 "ON"; REMAINING CHANNELS CONNECTED TO GND (SEE FIGURE 14).
 c. ALL CHANNELS DRIVEN EXCEPT CHANNEL 4, WHICH IS "ON."

Figure 16. ADG508AKN and ADG528AKN (Plastic DIPs) Crosstalk Results vs. Frequency



a. ALL CHANNELS DRIVEN EXCEPT CHANNEL 1, WHICH IS "ON."
 b. S4 DRIVEN; S3 "ON"; REMAINING CHANNELS CONNECTED TO GND (SEE FIGURE 14).
 c. ALL CHANNELS DRIVEN EXCEPT CHANNEL 4, WHICH IS "ON."

Figure 17. ADG508ABQ and ADG528ABQ (Cerdips) Crosstalk Results vs. Frequency



ALL CHANNELS DRIVEN EXCEPT CHANNEL 1, WHICH IS "ON."

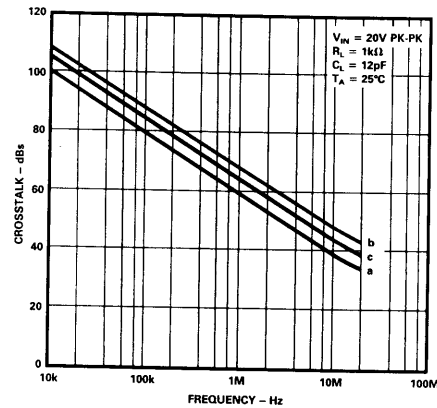
Figure 18. ADG508AKN and ADG528AKN (Plastic DIPs) Crosstalk Results vs. Frequency for Different R_L

ADG506A Series Results

Typical crosstalk plots for the ADG506A and ADG526A are shown in Figures 19 and 20. The ADG507A and ADG527A yield similar results except at high frequencies where the results would be marginally worse due to the lower C_D of these parts.

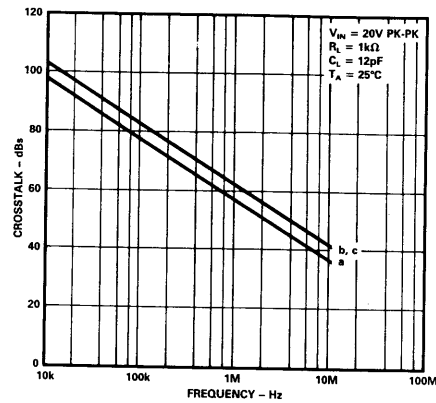
Since the ADG506A series has no analog input channel and output on adjacent pins, the results for this series surpass those for the ADG508A series. S8 is the channel nearest to the output, and therefore driving S8 with any other channel selected contributes most to poor crosstalk results.

In general, comments on the ADG508A series results apply for the ADG506A series also.



a. ALL CHANNELS DRIVEN EXCEPT CHANNEL 1, WHICH IS "ON."
 b. S8 DRIVEN; S7 "ON"; REMAINING CHANNELS CONNECTED TO GND (SIMILAR TO FIGURE 14).
 c. ALL CHANNELS DRIVEN EXCEPT CHANNEL 8, WHICH IS "ON."

Figure 19. ADG506AKN and ADG526AKN (Plastic DIPs) Crosstalk Results vs. Frequency



a. ALL CHANNELS DRIVEN EXCEPT CHANNEL 1, WHICH IS "ON."
 b. S8 DRIVEN; S7 "ON"; REMAINING CHANNELS CONNECTED TO GND (SIMILAR TO FIGURE 14).
 c. ALL CHANNELS DRIVEN EXCEPT CHANNEL 8, WHICH IS "ON."

Figure 20. ADG506ABQ and ADG526ABQ (Cerdips) Crosstalk Results vs. Frequency

COMMENTS

The results furnished in this application note are based on measurements from three fabrication lots. With the same conditions and device type, the results varied very little from lot to lot and from device to device. For example, the results for both OFF isolation and crosstalk varied by typically 1 dB only. For bandwidth, the variation in results was less than 0.2 MHz.