Data Sheet | August 2003 | FN1929.4

3MHz, BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output

The CA5260A and CA507.260 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5260 series circuits are dual versions of the popular CA5160 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected P-Channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5260 Series circuits operate at supply voltages ranging from 4.5V to 16V, or ±2.25V to ±8V when using split supplies.

The CA5260, CA5260A have guaranteed specifications for 5V operation over the full military temperature range of -55^{o}C to 125^{o}C.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
CA5260AM96 (5260A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA5260E	-55 to 125	8 Ld PDIP	E8.3
CA5260M (5260)	-55 to 125	8 Ld SOIC	M8.15
CA5260M96 (5260)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15

Features

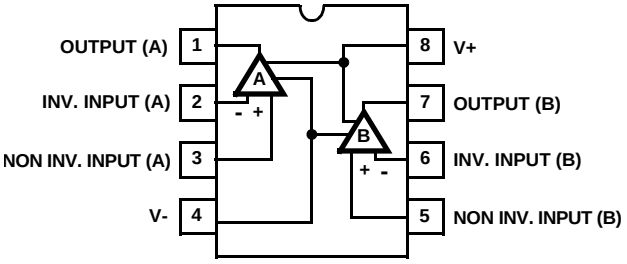
- MOSFET Input Stage provides
  - Very High Z_I = 1.5TΩ (1.5 x 10^{12}Ω) (Typ)
  - Very Low I_I = 5pA (Typ) at 15V Operation = 2pA (Typ) at 5V Operation
- Ideal for Single Supply Applications
- Common Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5260A, CA5260 Have Full Military Temperature Range Guaranteed Specifications for V+ = 5V
- CA5260A, CA5260 are Guaranteed to Operate Down to 4.5V for A_{OL}
- Fully Guaranteed to Operate from -55^{o}C to 125^{o}C at V+ = 5V, V- = GND

Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g., Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to 0V)
- Wien Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

Pinout

CA5260 (PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 16V
Differential Input Voltage 8V
Input Voltage . . . . . (V+ +8V) to (V- -0.5V)
Input Current 1mA
Output Short Circuit Duration (Note 1). . . . . Indefinite

Operating Conditions

Temperature Range. . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
PDIP Package	105
SOIC Package	157

Maximum Junction Temperature (Die) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA5260	CA5260A	
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T		3	3	MHz
Slew Rate	SR	$V_{OUT} = 2.5V_{P-P}$	5	5	V/µs
Transient Response		C_L = 25pF, R_L = 2kΩ (Voltage Follower)			
Rise Time	t_r		0.09	0.09	µs
Overshoot	OS		10	10	%
Settling Time (To <0.1%, $V_{IN} = 4V_{P-P}$)	t_S	C_L = 25pF, R_L = 2kΩ (Voltage Follower)	1.8	1.8	µs

Electrical Specifications

$T_A = 25^oC$, V+ = 5V, V- = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	V_O = 2.5V	-	2	15	-	1.5	4	mV
Input Offset Current	I_{IO}	V_O = 2.5V	-	1	10	-	1	10	pA
Input Current	I_I	V_O = 2.5V	-	2	15	-	2	15	pA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	70	85	-	80	85	-	dB
		V_{CM} = 0 to 2.5V	50	55	-	50	55	-	dB
Common Mode Input Voltage Range	V_{ICR}^+		2.5	3	-	2.5	3	-	V
	V_{ICR}^-		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	ΔV+ = 1V; ΔV- = 1V	70	84	-	75	84	-	dB
Large Signal Voltage Gain (Note 3)	A_{OL}	$R_L = \infty$, V_O = 0.5 to 4V	105	111	-	107	113	-	dB
		R_L = 10kΩ, V_O = 0.5 to 3.6V	80	86	-	83	86	-	dB
Source Current	I_{SOURCE}	V_O = 0V	1.75	2.2	-	1.75	2.2	-	mA
Sink Current	I_{SINK}	V_O = 5V	1.70	2	-	1.70	2	-	mA
Output Voltage	V_{OM}^+	$R_L = \infty$	4.99	5	-	4.99	5	-	V
	V_{OM}^-		-	0	0.01	-	0	0.01	V

Electrical Specifications $T_A = 25^oC$, V+ = 5V, V- = 0V **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	$V_{OM}+$	$R_L = 10k\Omega$	4.4	4.7	-	4.4	4.7	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
	$V_{OM}+$	$R_L = 2k\Omega$	3	3.4	-	3	3.4	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	$V_O = 0V$	-	1.60	2.0	-	1.60	2.0	mA
		$V_O = 2.5V$	-	1.80	2.25	-	1.80	2.25	mA

NOTE:

3. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at $R_L = 10k\Omega$.

Electrical Specifications $T_A = -55^oC$ to 125^oC, V+ = 5V, V- = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$V_O = 2.5V$	-	3	20	-	2	15	mV
Input Offset Current	I_{IO}	$V_O = 2.5V$	-	1	10	-	1	10	nA
Input Current	I_I	$V_O = 2.5V$	-	2	15	-	2	15	nA
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 1V	60	78	-	65	78	-	dB
		V_{CM} = 0 to 2.5V	50	60	-	50	60	-	dB
Common Mode Input Voltage Range	$V_{ICR}+$		2.5	3	-	2.5	3	-	V
	$V_{ICR}-$		-	-0.5	0	-	-0.5	0	V
Power Supply Rejection Ratio	PSRR	$\Delta V+ = 1V$; $\Delta V- = 1V$	60	65	-	62	65	-	dB
Large Signal Voltage Gain (Note 4)	A_{OL}	$R_L = \infty$, V_O = 0.5 to 4V	70	78	-	70	78	-	dB
		$R_L = 10k\Omega$, V_O = 0.5 to 3.6V	60	65	-	60	65	-	dB
Source Current	I_{SOURCE}	$V_O = 0V$	1.3	1.6	-	1.3	1.6	-	mA
Sink Current	I_{SINK}	$V_O = 5V$	1.2	1.4	-	1.2	1.4	-	mA
Output Voltage	$V_{OM}+$	$R_L = \infty$	4.99	5	-	4.99	5	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
	$V_{OM}+$	$R_L = 10k\Omega$	4.2	4.4	-	4.2	4.4	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
	$V_{OM}+$	$R_L = 2k\Omega$	2.5	2.7	-	2.5	2.7	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
Supply Current	I_{SUPPLY}	$V_O = 0V$	-	1.65	2.2	-	1.65	2.2	mA
		$V_O = 2.5V$	-	1.95	2.35	-	1.95	2.35	mA

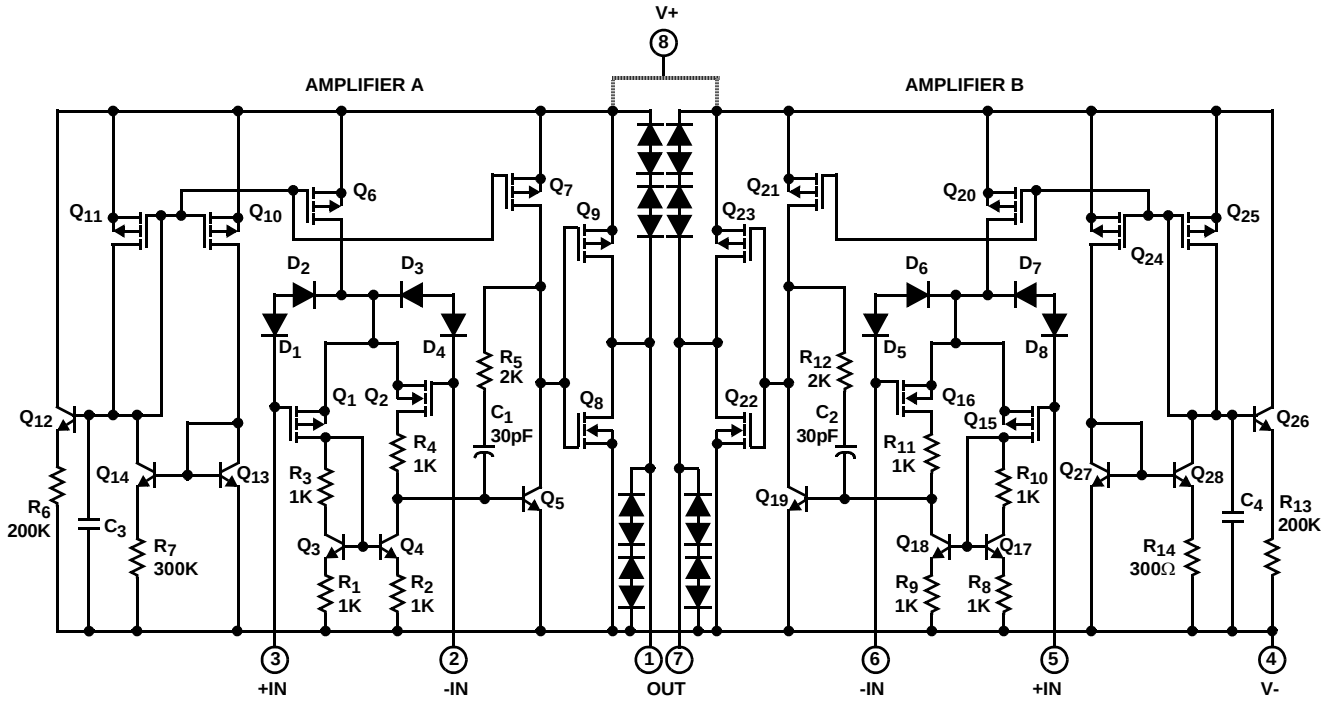
NOTE:

4. For V+ = 4.5V and V- = GND; V_{OUT} = 0.5V to 3.2V at $R_L = 10k\Omega$.

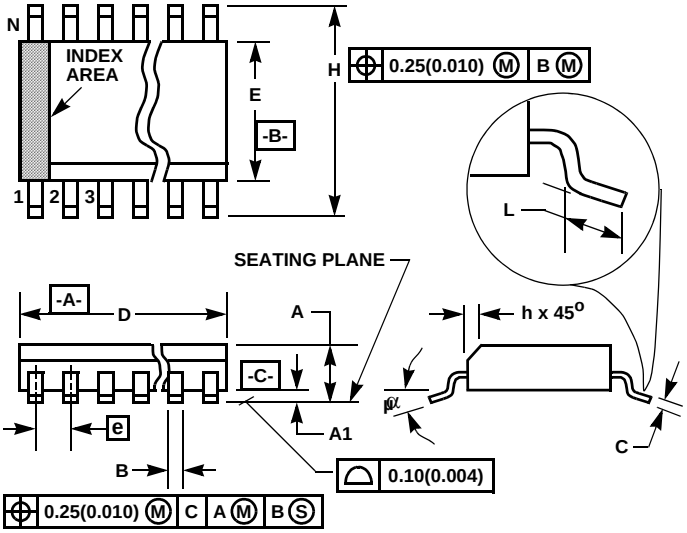
Electrical Specifications Each Amplifier at $T_A = 25^oC$, V+ = 15V, V- = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA5260			CA5260A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{IO}	$V_S = \pm 7.5$	-	6	15	-	2	5	mV
Input Offset Current	I_{IO}	$V_S = \pm 7.5$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	$V_S = \pm 7.5$	-	5	50	-	5	30	pA
Large Signal Voltage Gain	A_{OL}	$V_O = 10V_{P-P}$, $R_L = 10k\Omega$	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common Mode Rejection Ratio	CMRR		70	90	-	80	95	-	dB
Common Mode Input Voltage Range	V_{ICR}		10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V\pm$	PSRR	$V_S = \pm 7.5$	-	32	320	-	32	150	μV/V
Maximum Output Voltage	$V_{OM}+$	$R_L = 10k\Omega$	11	13.3	-	11	13.3	-	V
	$V_{OM}-$		-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	$R_L = \infty$	14.99	15	-	14.99	15	-	V
	$V_{OM}-$		-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ (Source)	$V_O = 7.5V$	12	22	45	12	22	45	mA
	$I_{OM}-$ (Sink)		12	20	45	12	20	45	mA
Total Supply Current, $R_L = \infty$	I+	V_O (Amp A) = 7.5V V_O (Amp B) = 7.5V	-	9	16.5	-	9	16.5	mA
		V_O (Amp A) = 0V V_O (Amp B) = 0V	-	1.2	4	-	1.2	4	mA
		V_O (Amp A) = 0V V_O (Amp B) = 7.5V	-	5	9.5	-	5	9.5	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	8	-	-	6	-	$\mu V/^oC$
Crosstalk		f = 1kHz	-	120	-	-	120	-	dB

Schematic Diagram



Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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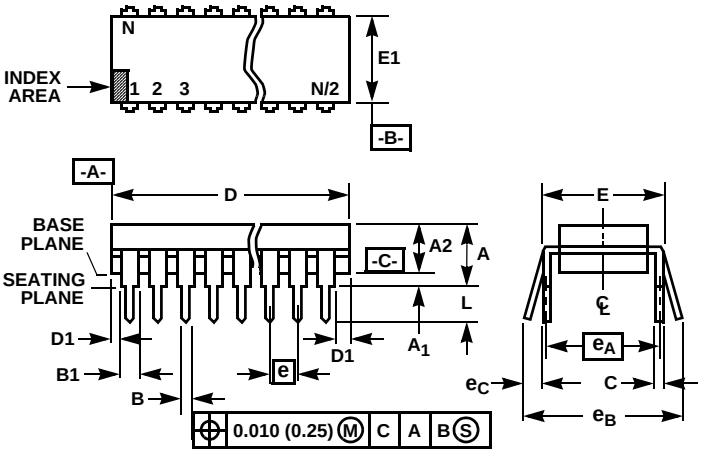
Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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